TECHNICAL BULLETIN

No. TB 11-6690-252-10-4

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 15 January 1979

SUPPLEMENTARY OPERATION INSTRUCTIONS

TEST SET, INTEGRATED CIRCUIT CARD

TESTERS AN/USM-371 AND AN/USM-371A

(TEST PROGRAMS FOR AUTODIN

RRINTED CIRCUIT CARDS

NO. SM-E-546587 THROUGH SM-E-546840)

REPORTING OF ERRORS

You can improve this bulletin by recommending improvements **using** DA Form 2028-2, Fill out the form and forward it to the **Commander, US Army Communications and** Electronics Materiel **Readiness Command, ATTN: DRSEL-ME-MQ**, Fort Monmouth, NJ 07703.

A reply will be furnished directly to you.

1. Purpose This technical bulletin provides supplemntary instructions **in** the test programs and associated data for troubleshooting AUTODIN printed circuit cards No. SM-E-546587 **through** SM-E-546840 using Test Set. Integrated Circuit Card Tester AN/USM-371 and AN/USM-371A.

NOTE:

In this bulletin, the following test sets are referenced by **the** indicated manufacturer's model number:

Nomenclature	Mode. Numbe
AN/USM-371	Model ICT-102
AN/USM-371A	Model ICT-103

2. Test Procedures. Refer to the general instructions to become familiar with the basic data required for troubleshooting the faulty printed circuit card. Locate the schematic diagram and test data that pertain to the faulty card. Operate the test set to isolate the fault as described in the operating procedures.

06-000129
VOL. 2 of 2

Dynatronics Products

PC CARD TEST PROGRAMS
for the
MODEL ICT- 102 and ICT- 103
PRINTED CIRCUIT CARD TESTER

INTEGRATED CIRCUIT CARD TEST SET
AN/USM-371 and AN/USM371A
used for
AUTODIN PC CARDS
SM-E-546 587 through SM-E-546 840

PROGRAM MANUAL

GENERAL DYNAMICS
Electro Dynamic Division

LIST OF EFFECTIVE PAGES

TOTAL NUMBER OF PAGES IS 99 AS FOLLOWS:

Page No.	Issue	Page No.	Issue	Page No.	Issue	Page No.	Issue
Title	Original						
A	Original						
i- ii	Original						
1 through 95	Original						

* The asterisk indicates pages revised, added or deleted by the current change.

TABLE OF CONTENTS

	Page
General Description	1
Card Tester Schematic **or** Logic Diagram **Markings**	2
Card Tester Waveform Markings	3
Model ICT-102 Operating Procedures	3
Model ICT-103 Operating Procedures	6
Special Considerations	
Jumpers	8
+5V EXT Power **Supply** Adjustment	8
Printed Circuit Card Adapters	10
Printed Circuit Card Adapter MX-9098/USM-371.	11
Printed Circuit Card Adapter MX-9090/USM-371.	12
Printed Circuit Card Adapter MX-9091/USM-371.	13
Printed Circuit Card Adapter MX-9092/USM-371.	14
Printed Circuit Card Adapter MX-9093/USM-371.	15
Printed Circuit Card Adapter MX-9094/USM-371.	16
Printed Circuit Card Adapter MX-9095/USM-371.	17
Printed Circuit Card Adapter MX-9096/USM-371.	18
Printed Circuit Card Adapter MX-9097/USM-371.	19
Printed Circuit Card Assembly Numbers	20-95
SM-E-546587	20,21
SM-E-546590	22,23,24,25
SM-E-546593	26,27,28,29
SM-E-546596	30,31

TABLE OF CONTENTS (CONT'D)

	Page
SM-E--546599	32,33
SM-E-546602	34,35
SM-E-546605	36,37,38,39
SM-E-546614	40,41,42,43
SM-E-546620	44,45
SM-E-546623	46,47
SM-E-546626	48,49
SM-E-546629	50,51
SM-E-546632	52,53
SM-E-546635	54,55,56,57
SM-E-546638	58,59,60,61
SM-E-546641	62,63
SM-E-546644	64,65,66,67
SM-E-546647	68,69,70,71
SM-E-546653	72,73
SM-E-546656	74,75
SM-E-546659	74,75
SM-E-546662	76.77
SM-E-546807	78,79
SM-E-546810	80,81,82,83
SM-E-546831	84,85,86,87,88,89
SM-E-546837	92, 93
SM-E-546840	94-95

LIST OF ILLUSTRATIONS

Figure		Page
1	Printed Circuit Card Testers (100 Series)	1
2	Model ICT-102 Waveform Sheet Example	4
3	Model ICT-103 Waveform Sheet Example	.6
4	Typical RC Network	9
5	Voltage Tolerance Versus Time Delay Chart	9
6	Printed Circuit Card Adapter MX-9089/USM-371 (23 Pin Anelex)	11
7	Printed circuit Card Adapter MX-9090/USM-371 (44/48 Pin Anelex)	12
8	Printed Circuit Card Adapter MX-9091/USM-371 (22 Pin SN-394 Red)	13
9	Printed Circuit Card Adapter MX-3092/USM-371.. (26 Pin SN-394 Black)	14
10	Printed Circuit Card Adapter MX-9093/USM-371 (22 Pin MD-674)	15
11	Printed Circuit Card Adapter MX-9094/USM-371.. (43/86 Pin FGC)	16
12	Printed Circuit Card Adapter MX-9095/USM-371 (60 Pin TCU)	17
13	Printed Circuit Card Adapter MX-9096/USM-371 (46 Pin GDE)	18
14	Printed Circuit Card Adapter MX-9097/USM-371 (25 Pin FGC)	19

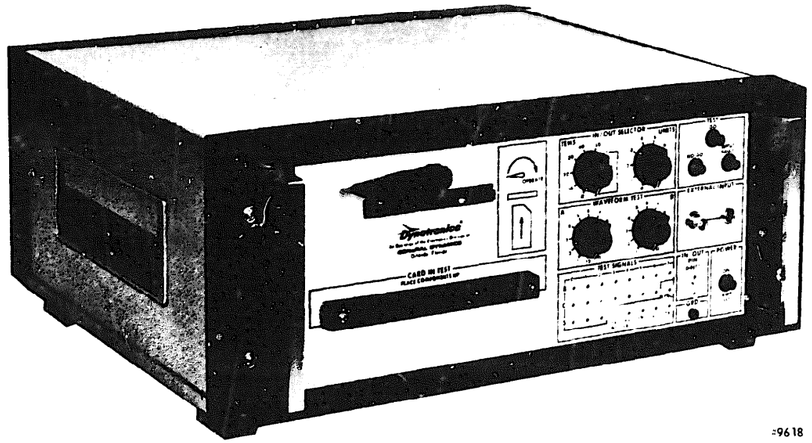
LIST OF TABLES

Table		Page
1	Printed Circuit Card Adapters	10
2	Printed Circuit Card Adapter MX-9089/USM-371 Pin Cross Reference	11
3	Printed Circuit Card Adapter MX-9090/USM-371 Pin Cross Reference	12
4	Printed Circuit Card Adapter MX-9091/USM-371 Pin Cross Reference	13
5	Printed Circuit Card Adapter MX-9092/USM-371 Pin Cross Reference	14
6	Printed Circuit Card Adapter MX-9093/USM-371 Pin Cross Reference	15
7	Printed Circuit Card Adapter MX-9094/USM-371 Pin Cross Reference	1 6
8	Printed Circuit Card Adapter MX-9095/USM-371 Pin Cross Reference	17
9	Printed Circuit Card Adapter MX-9096/USM-371 Pin Cross Reference	18
10	Printed Circuit Card Adapter MX-9097/USM-371 Pin Cross Reference	19

GENERAL DESCRIPTION

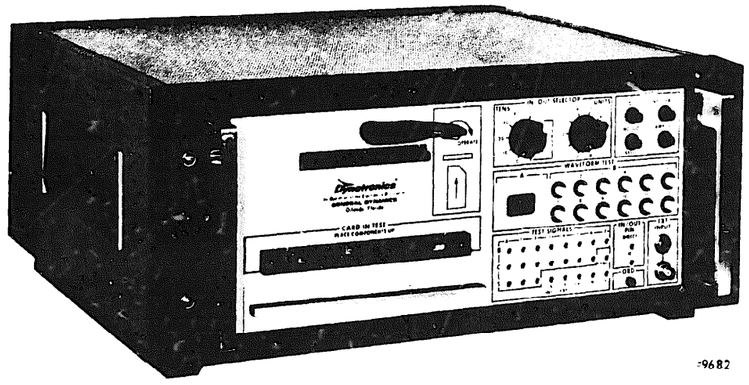
Dynatronics Printed Circuit Card tester models ICT-102 and ICT-103 provide the capability for dynamically testing virtually any logic family on a visual basis. Punched Hollerith cards contain individual programs which eliminate elaborate test hook-ups normally found during testing operations. No external test equipment is necessary because complete dynamic tests are performed by the Card Tester each time an individual program card is inserted into the card reader. All conditions (signal generation, power distribution, grounding, loading, test rates, etc.) are **controlled by the program card and all circuits are fully tested** by **following a simple set of instructions and observing the GO/NO-GO and FAULT indicator lamps on the front panel . These instructions are provided in the following paragraphs.**

Differences in the two models (ICT-102 and ICT-103) are illustrated in figure 1, Basically the card testers function alike with the main differences being in operator switch setting procedures. The model ICT-102 Card Tester uses rotary switches for selecting circuit under test output signal GO/NO-GO test parameters whereas the model ICT-103 Card Tester features pushbuttons in place of the rotary switches. Individual card test documentation provided in this manual can **be used for either model** Card Tester.



-9618

MODEL ICT-102 CARD TESTER



-9682

MODEL ICT-103 CARD TESTER

Figure 1. Printed Circuit Card Testers (100 Series)

CARD TESTER SCHEMATIC OR LOGIC DIAGRAM MARKINGS

Each schematic or logic diagram associated with inldividual programmed cards are marked such that pertinent information related to signal routing, power distribution, and other test requirements are readily available to the test technician. Markings and symbols normally found on schematic or logic diagrams are listed below:

a. Parenthesis - Used to enclose test information such as pin numbers and test signals generated by the card tester and routed to the card- under-test via the card reader, i.e., (4) indicates that this pin connects to the card tester CARD IN TEST connector, pin 4; (+CO) indicates that test signal +CO is Connected to the card-under-test via the card reader.

b. Symbol (H) - Placed adjacent to schematic wiring which remain at a high logic level throughout the test. A high logic level is defined as the upper level of the signal voltage levels.

c. Symbol (L) - Placed adjacent to schematic wiring which remain at a low logic level throughout the test. A low logic level is defined as the lower level of the signal voltage levels.

Nate

All points not labeled (H) or (L) are dynamic i.e., are switching during the test.

d. -++++++++++++ - This symbol indicates input or output lines which are not tested by the card tester test program. On cards which are tested by two programs, the symbol indicates that the input or output line is not tested by either program.

e. (GRD) Symbol - Indicates that DC power ground from the card tester is applied to the card-under-test at this point.

f. (+VCC) Symbol - Independent +5 ±0.5 volt power supply internal to the card tester used for supplying +Vcc to the card-under-test via the card test program. This power supply, +5 EXT, is adjusted from the rear panel of the card tester.

g. ±v, +V -V Symbols - These symbols indicate which of the three program-mable power supplies are connected to the card-under-test. The output voltage values for the programmable power supplies are located on the waveform sheet in the TEST PARAMETERS table.

h. (NC) Symbol - Indicates that there is no connection made between the referenced point on the card-under-test and the card tester,

These markings are located on the schematic drawings where applicable and are defined in the TEST LEGEND contained on each schematic. Definitions for the above markings apply to both the ICT-102 and ICT-103 Card Tasters.

CARD TESTER WAVEFORM MARKINGS

Several symbols are used on the waveform charts to indicate special procedures required while testing a particular printed circuit card. These symbols and/& special instructions are located in the notes at the bottom of each waveform chart. Before proceeding with any test it is required that the notes be read and special instructions be carried out. For example, the notes may indicate that the Card Tester +5 volt external power supply be adjusted to +4.5 volts prior to testing the printed circuit card in question. In this case the printed circuit card could be damaged if the power supply had been adjusted to +5.5 volts for the preceeding test. Typical notes and symbols are described below:

a. Asterisk * Symbol - This symbol when placed adjacent to a pin number (either input or output pin) on the waveform chart indicates that the signal on that pin is inverted with respect to the waveform shown. Typically these symbols are located in the INPUT PINS and OUTPUT PINS columns of the waveform chart.

b. # Symbol - Indicates that no further edges are present in the output signal under test and the output is tested according to the steps for the model of Card Tester in use.

c. Encircled Output Pins - Encircled output pins are the more significant outputs that when tested check the majority of the circuits on the card-under-test. These output pins should be tested first to determine the general status of the card being tested. For example, when testing a multiple stage shift register with individual stages brought out on pins, the last stage of the shift register would be encircled and tested before the individual stages were tested. In this manner it is determined that the card is functionally operational after checking a single output pin.

MODEL ICT-102 OPERATING PROCEDURES

Following is the step-by-step procedure for performing dynamic test analysis on printed Circuit cards programmed for the model ICT 102 Card Tester. These instructions pertain to all printed circuit cards: specific instructions peculiar to individual printed circuit cards undergoing tests are listed as notes on the appropriate waveform sheet. Waveform sheets for individual printed circuit cards are contained in this volume. Before proceeding with any test, the operator must read the notes contained on the waveform sheet and follow any specific instructions first. In addition the necessary card adapters, card extender cables, and programmable load boards should be inserted in the Card Tester to accommodate the card to be tested. The steps listed below provide the necessary information for successful diagnostic testing of all printed circuit cards programmed for testing with the ICT-102.

a. Refer to the appropriate card under test schematic or logic diagram and corresponding waveform sheet. On the waveform sheet, locate the notes and follow the instructions pertinent to the operator. Typically, the notes are located along the bottom edge of the waveform sheet.

b. Insert the PC card adapter and/or extender cable (if required) into the CARD IN TEST connector on the front panel of the Card Tester.

c. Insert the printed circuit card to be tested into the card adapter with the component side facing up.

d. Locate the corresponding card under test program card and insert it into the card reader slot as depicted on the front panel of the Card Tester. Push the program card into the card reader slot until there is a noticeable resistance felt against the test card. Move the card reader handle clockwise until it is in the full closed position.

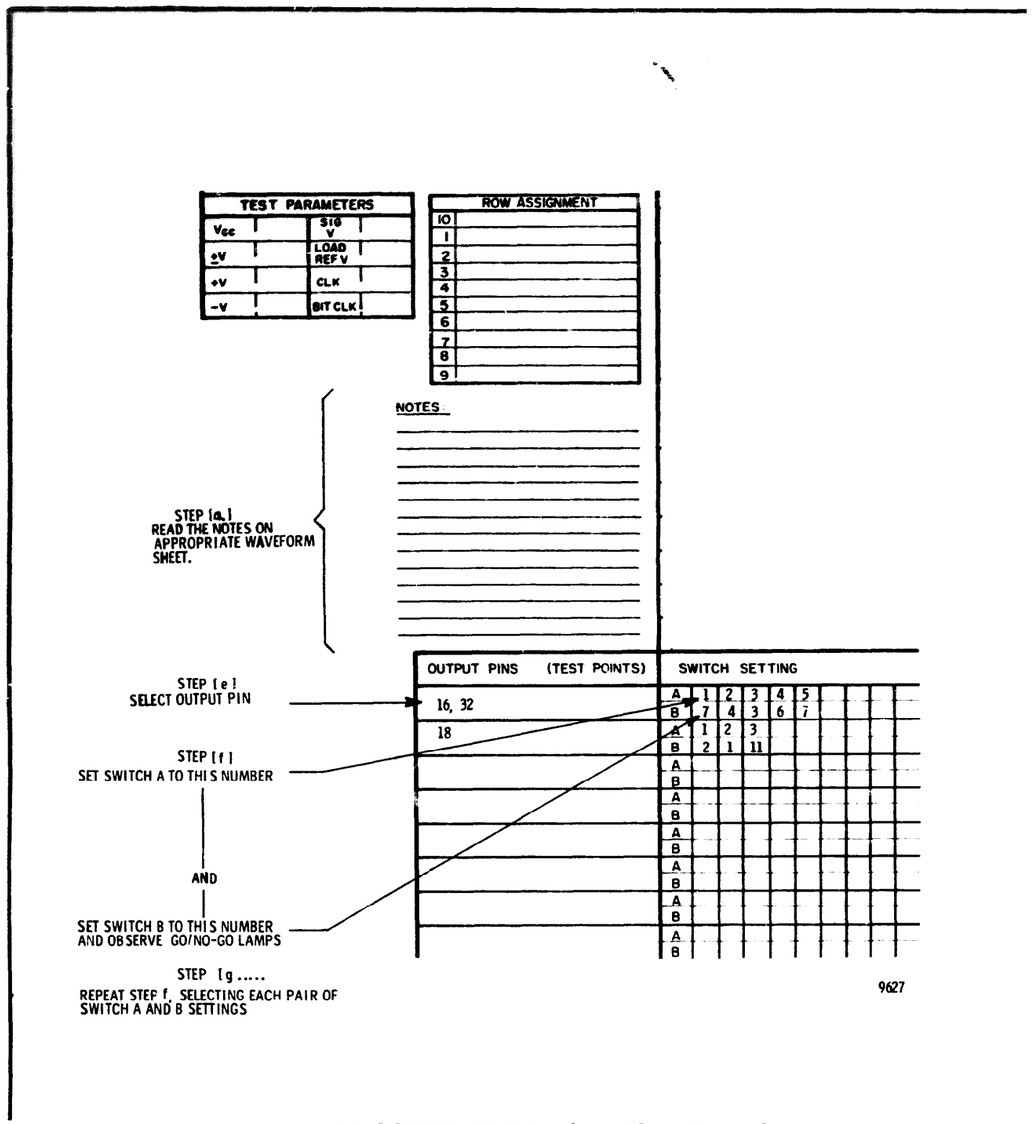


Figure 2. Model ICT-102 Waveform Sheet Example

Note

When initially energized, the Card Tester INPUT FAULT indicator is illuminated. Resetting the Card Tester should clear the INPUT **PAULT indicator.** If the INPUT **FAULT indicator is** not **extinguished after resetting the Card Tester, a true input fault is present in the card-under-test** and should be **corrected before continuing.**

e. Select the output pin to be tested on the front panel IN/OUT SELECTOR switches (S2 and S3). Figure 2 shows a typical example of an output pin (pin 16) and its location on the waveform chart.

f. Set WAVEFORM TEST switch A to the first number shown under tne SWITCH SETTING heading which corresponds to the selected output pin on the waveform chart. As shown in figure 2, the number 1 would be selected by switch A.

g. Place WAVEFORM TEST switch B to the first number adjacent to SWITCH SETTING B which corresponds to the selected output pin.

h. Observe the three TEST indicators on the front panel and determine the outcome of the circuit being tested. The two possible indications are explained below:

1. GO indicator lights green - circuit being tested checks good for this measurement and the operator should continue with the next step.

2. NO-GO indicator lights red - circuit being tested does not meet the output requirements for the programmed test. **Recheck the switch settings to ensure that there has been no operator' error and then make the necessary notations on the card in test paper work for follow-up maintenance.**

i, Place WAVEFORM TEST switches A and B to the nex pair of SWITCH SETTINGS, shown on the waveform **chart, and observe the TEST indicators as in the previous step.** Continue this procedure until **all settings for a given** output pin have been carried out and all test indications have been GO.

Note

A # symbol in the last "B" **switch** setting position indicates that a NO-GO indication should be observed for all "B" switch settings (1 through 12). A GO indication in any of these positions indicates a malfunction (more edges than required).

j. Change both IN/OUT SELECTOR switches to the next output pin number located on the waveform chart either adjacent to the output just tested or, if there is no adjacent number, to the next output pin number directly below the output pin just tested.

k. Place WAVEFORM TEST switches A and B to each pair of corresponding SWITCH SETTING numbers. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO. Repeat **steps** (j.) and (k.) until all output pins and corresponding SWITCH SETTINGS have **been** tested.

1. Rotate the card **reader** handle counter-clockwise **to the** full open position, remove the Program **card from the** card reader **slot and** insert **the test card into the appropriate plastic card** holder.

m. Determine whether or not the card under test requires additional testing **using another program test card. If additional testing** is required, repeat steps **(a.) through (m.) for the additional test** (s) . If no further testing is required, **remove the tested printed circuit card from** the card adapter.

MODEL ICT-103 OPERATING PROCEDURES

Following is the step-by-step procedure for performing dynamic test analysis on printed circuit cards programmed for the model ICT-103 Card Tester. These instructions pertain to all printed circuit cards: specific instructions peculiar to individual printed circuit cards undergoing tests are listed as notes on the appropriate waveform sheet. Waveform sheets for individual printed circuit cards are contained in this volume. Before proceeding with any test, the operator must read the notes contained on the waveform sheet and follow any specific instructions first. In addition the necessary card adapters, card extender cables, and programmable load boards should be inserted in the Card Tester to accommodate the card to be tested. The steps listed below provide the necessary information for successful diagnostic testing of all printed circuit cards programmed for testing with the ICT-103.

a. Refer to the appropriate card under test schematic or logic diagram and corresponding waveform sheet. On the waveform sheet, locate the notes and follow the instructions pertinent to the operator. Test notes are normally located along the bottom edge of the waveform sheet.

b. Insert the PC card adapter and/or extender cable (if required) into the CARD IN TEST connector on the front panel of the Card Tester.

C. Insert the printed circuit card to be tested into the card adapter with the component side facing up.

d. Locate the corresponding card-under-test program card and insert it into the card reader slot as depicted on the front panel of the Card Tester. Push the program card into the card reader slot until there is a noticeable resistance felt against the test card. Move the card reader handle clockwise until it is in the full closed position.

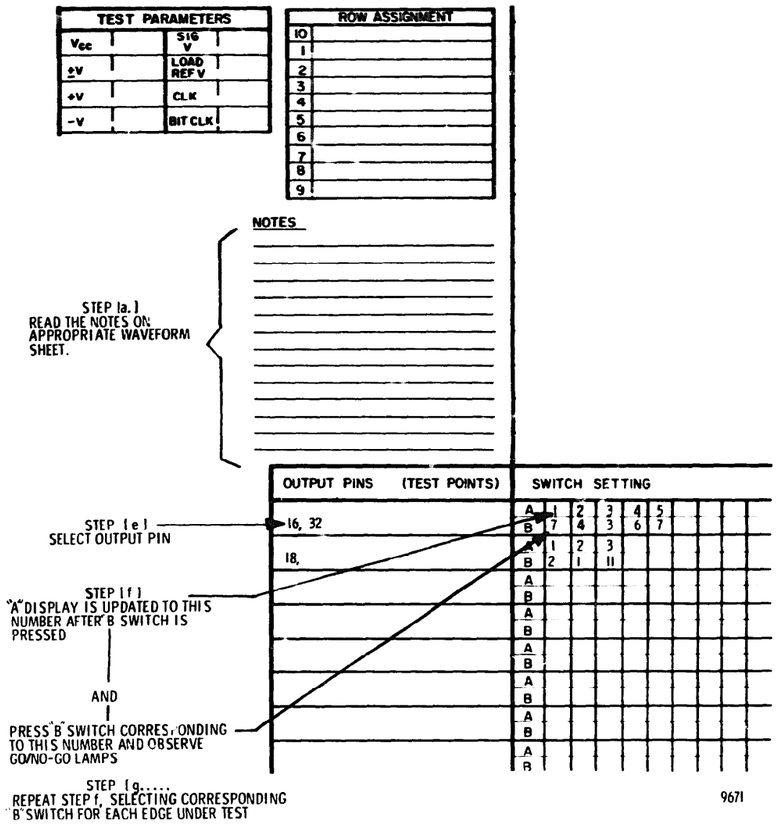


Figure 3. Model ICT-103 Waveform Sheet Example

Note

If the INPUT FAULT indicator is lit, press the RESET switch. If the INPUT FAULT indicator is not extinguished after resetting the Card Tester, a true input fault is present in the card-under-test and should be corrected before continuing.

e. Select the output pin to be tested on the front panel IN/OUT SELECTOR switches (S2 and S3). Figure 3 shows a typical example of an output pin (pin 16) and its location on the waveform chart.

f. WAVEFORM TEST "A" display should read 0 (left digit blank). If the "A^{am} display does not read zero, press the reset switch/indicator.

g. Press the WAVEFORM TEST "B" switch corresponding to the first number adjacent to SWITCH SETTING B (figure 3) which corresponds to the selected output pin (switch number 7 in this example). WAVEFORM TEST display "A" changes to (01).

h. Observe the three TEST indicators on the front panel and determine the outcome of the circuit being tested. The two possible indications are explained below:

1. GO indicator lights green - circuit being tested checks good for this measurement and the operator should continue with the next step.

2. NO-GO indicator lights red - circuit being tested does not meet the output requirements for the programmed test. Recheck the switch settings to ensure that there has been no operator error and then make the necessary notations on the card in test paper work for follow-up maintenance.

i. Press WAVEFORM TEST switch B which corresponds to the next B SWITCH SETTING, shown on the waveform chart, and observe the TEST indicators as in the previous step. Each time a B switch is press the A display is incremented one count. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO.

j. Change both IN/OUT SELECTOR switches to the next output pin number located on the waveform chart either adjacent to the output just tested or, if there is no adjacent number, to the next output pin number directly below the output pin just tested.

Note

A # symbol-in the last "B" switch setting position indicates that a GO test result should occur after "B" switch "#" is depressed. If a NO-GO indication is observed after pressing "B" switch "#", the circuit being tested has malfunctioned.

k. Press WAVEFORM TEST switch B for each pair of corresponding SWITCH SETTING numbers. Continue this procedure until all settings for a given OutPut pin have been carried out and all test indications have been GO. Repeat steps (j.) and (k.) until all output pins and corresponding SWITCH SETTINGS have been tested.

1. Rotate the card reader handle counter-clockwise to the full open position, remove the program card from the card reader slot and insert the test card into the appropriate plastic card holder.

m. Determine whether or not the card under test requires additional testing using another program test card. If additional testing is required, repeat steps (a.) through (m.) for the additional test (s) . If no further testing is required, remove the tested printed circuit card from the card adapter.

Note

In some instances, the GO/NO-GO test documentation may skip "A" display counts to enable the operator to ignore "don't care" transitions in the waveform under test. For example, consider the following:

A	1	2	3	4	5	6	7
B	6	9	NT	NT	3	6	10

Where NT = NO TEST

The operator would press the "B" switches in the following sequence: B-6 (A=1), B-9 (A=2), B-3 three times (steps A to count 5) B-6 (A=6), B-10 (A=7) .

SPECIAL CONSIDERATIONS

JUMPERS

Jumpers are required occasionally while performing tests on printed circuit cards for bypassing passive components or otherwise routing DC voltages within the card-under-test. These jumpers should be carefully placed on the card-under-test prior to inserting the program card (energizing the Card Tester) into the Card Tester and should be checked to ensure proper placement. Information concerning placement of jumpers is located in the notes at the bottom of the appropriate waveform test diagram and on the schematics or logic diagrams.

+ 5V EXT POWER SUPPLY ADJUSTMENT

Four power supply output voltages are available in the Card Tester which can be applied to the card-under-test. Three of these power supplies are controlled by the program test card and the fourth, the +5 Volt EXT power supply, is adjusted by the operator according to the individual test programs. When adjusting the +5V EXT power supply to accommodate different printed circuit card families, care should be taken to adjust the output voltage within ± 100 millivolts of the recommended voltage. Exceeding the 100 millivolt tolerance can cause erroneous readings on the Card Tester GO/NO-GO indicators, as described below.

Erroneous readings caused by maladjusted power supply voltages is normally due to the RC timing circuits present on many cards. A large voltage variation in either direction will cause a significant change in the duration of the timed interval, and may result in an erroneous "B" switch count. This phenomena is illustrated in Figure 4, along with the timing variations imposed by the tolerances on the resistor and capacitor values. The curves were generated for the circuit shown in figure 4. The switching threshold of gate Y was found

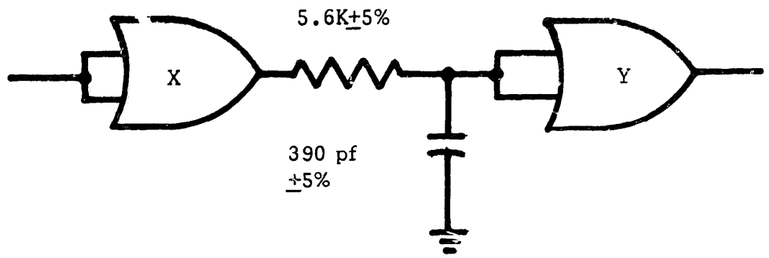


Figure 4. Typical RC Network

to remain nearly constant at approximately 2.0 volts as the supply voltage was varied from 4 ,50 to 5 .00 volts.

It is seen-in Figure 5 that with Vcc = 4.75 and nominal RC values, Gate Y will switch 1.68 usec after the‘ output of Gate X goes to the high state. With VCC = 5.00 and the resistor and capacitor values at the low end of the tolerance range, Gate Y will delay 1.43 usec before switching. With Vcc = 4.50 and the timing components at the high end of the tolerance range, Gate Y will delay 2.05 usec before switching. Thus. it is seen that for curves A and B, a “B“ switch count of 2 would be obtained; while an erroneous “B" switch count of 3 would be obtained for the conditions represented by curve C.

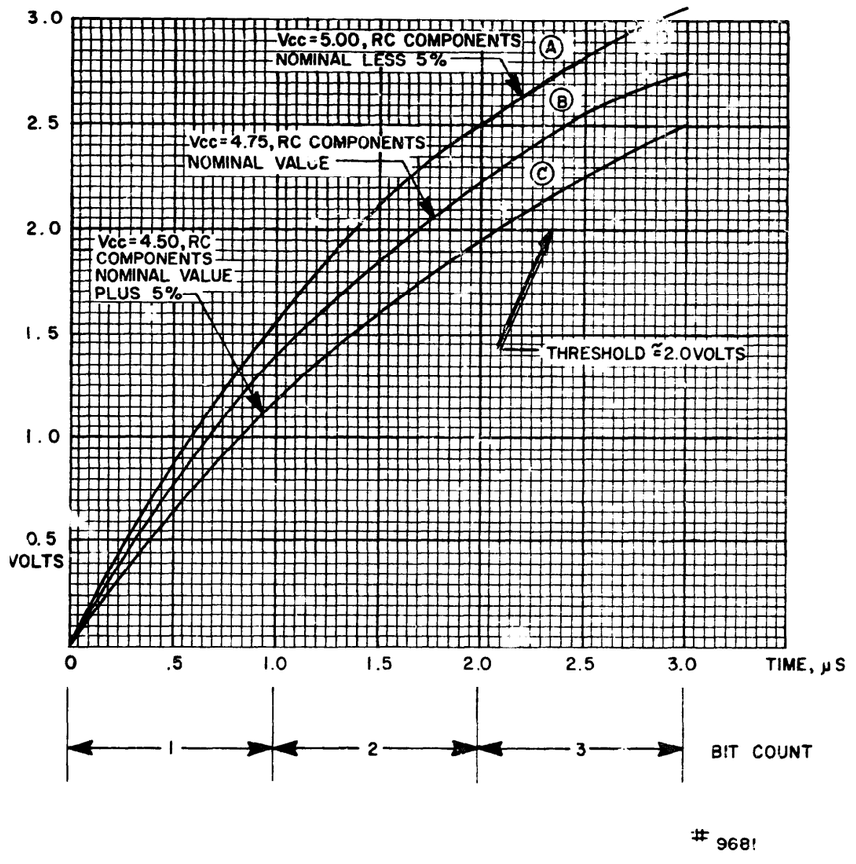


Figure 5. Voltage Tolerance Versus Time Delay Chart

For cases where the time delay circuit is isolated from other circuitry it would usually be possible to program around the problem discussed above. However on many cards, several timing circuits operate in series such that while one programming technique may provide a wide margin of safety for one circuit in the series, it may reduce the margin **of safety for another** timing circuit in the series. **Therefore** it is desirable to reduce the magnitude of error of the controllable **variables such as supply voltage which determine the duration of the timed intervals.**

Note

The above conditions also affect the pulse duration of slivers (spikes) noted in some program waveforms. These spikes are not tested by the Card Tester (too narrow for detection) and are not critical with respect to the logic circuit operation. In most cases the spikes are less than l0 nanoseconds in duration and in some cases are hardly discernable from one Card Tester to the next.

PRINTED CIRCUIT CARD ADAPTERS

Several printed circuit card adapters are available to interconnect between the Card Tester and various printed circuit card families contained in this manual. Following is a cross-reference table of the individual card adapters and associated printed circuit card family. Pin number cross-reference and **card adapter identification** for individual PC card adapters are provided in the following tables and illustrations.

Table 1. Printed Circuit Card **Adapters**

DYNATRONICS PART NO.	MILITARY NOMENCLATURE	ADAPTS CARD TESTER TO:
12-890051	**MX-9089/USM-371**	23 Pin Anelex
12-890052	MX-9090/USM-371	44/88 Pin Anelex
12-890053	**MX-909l/USM-371**	22 Pin SN-394 (RED)
12-890054	MX-9092/USM-371	26 Pin SN-394 (BLACK)
12-890056	MX-9093/USM-371	22 Pin MD-674
12-890059	MX-9094/USM-371	43/86 Pin FGC
12-890055	MX-9095/USM-371	60 Pin TCU
12-890050	MX-9096/USM-371	46 Pin GDE
12-890058	MX-9097/USM-371	25 Pin FGC

Table 2. Printed Circuit Card Adapter MX-9089/USM-371
Pin Cross Reference

ADAPTER MX-9089/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9089/USM-371	CARD TESTER PIN NUMBER
1	46	12	35
2	45	13	34
3	44	14	33
4	43	15	32
5	42	16	31
6	41	17	30
7	40	18	29
8	39	19	28
9	38	20	27
10	37	21	26
11	36	22	25
		23	24

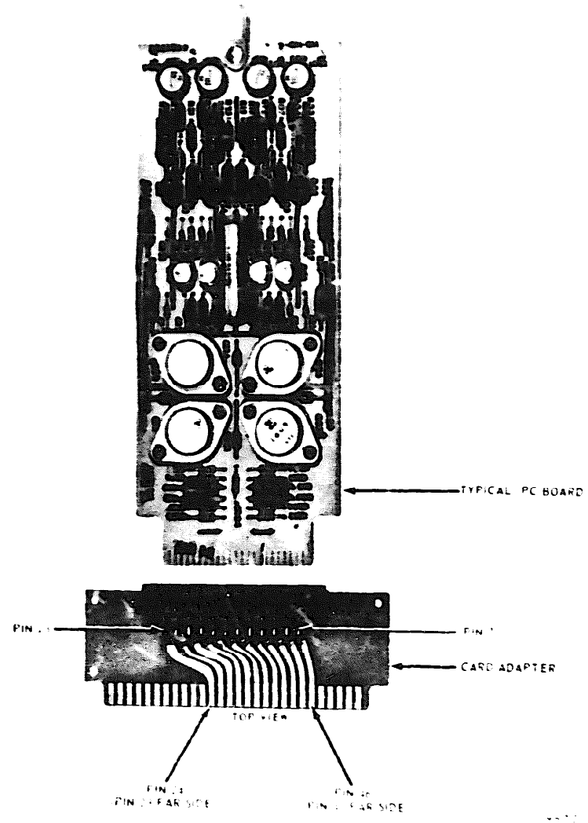


Figure 6. Printed Circuit Card Adapter MX-9089/USM-371
(23 Pin Anelex)

Table 3. Printed Circuit Card Adapter MX-9090/USM-371 Pin Cross Reference

ADAPTER MX-9090/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9090/USM-371	CARD TESTER PIN NUMBER
1	55	23	36
2	53	24	34
3	51	25	32
4	49	26	30
5	47	27	28
6	45	28	26
7	43	29	24
8	41	30	22
9	39	31	20
10	37	32	18
11	35	33	16
12	33	34	14
13	31	35	12
14	29	36	10
15	52	37	8
16	50	38	6
17	48	39	4
18	46	40	2
19	44	41	54
20	42	42	
21	40	43	56
22	38	44	

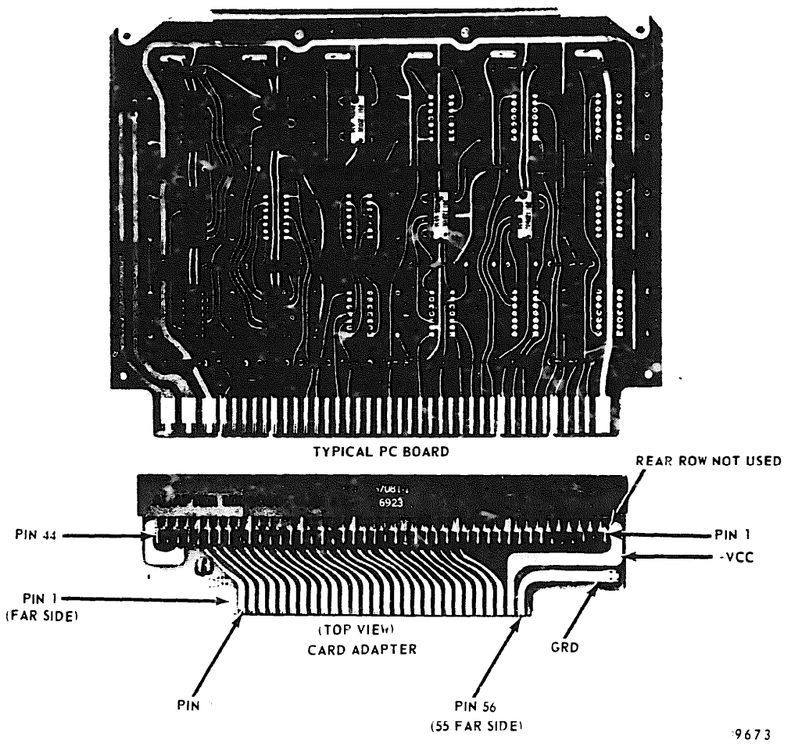


Figure 7. Printed Circuit Card Adapter MX-9090/USM-371 (44/88 Pin Anelex)

Table 4. Printed Circuit Card Adapter MX-9091/USM-371
Pin Cross Reference

ADAPTER MX-9091/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9091/USM-371	CARD TESTER PIN NUMBER
1	22	12	11
2	21	13	10
3	20	14	9
4	19	15	8
5	18	16	7
6	17	17	6
7	16	18	5
8	15	19	4
9	14	20	3
10	13	21	2
11	12	22	1

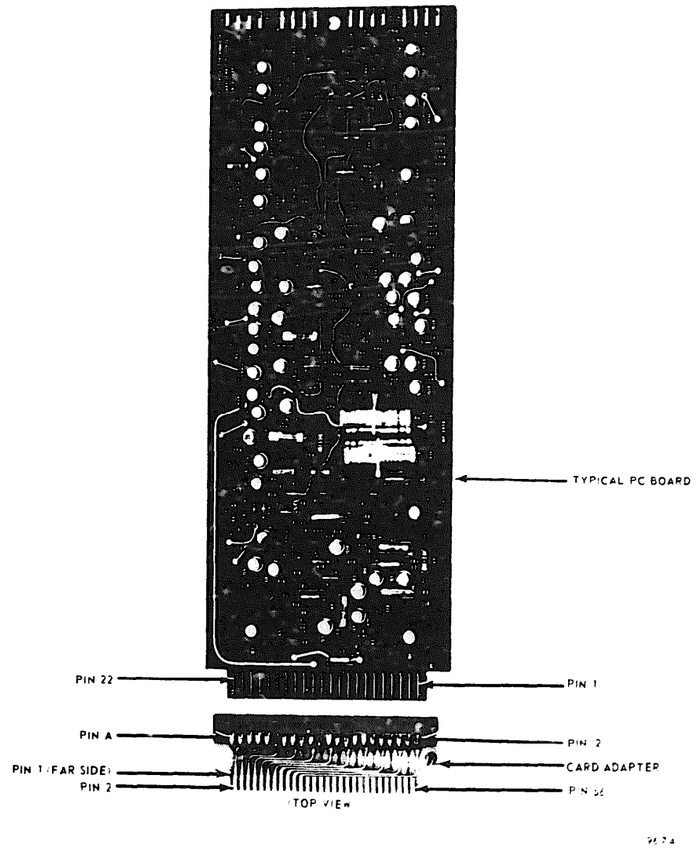


Figure 8, Printed Circuit Card Adapter MX-9091/USM-371
22 Pin SN-394 (Red)

Table 5. Printed Circuit Card Adapter MX-9092/USM-371 Pin Cross Reference

ADAPTER MX-9092/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9092/USM-371	CARD TESTER PIN NUMBER
1	52	29	26
2	51	30	25
3	50	31	24
4	49	32	23
5	48	33	22
6	47	34	21
7	46	35	20
8	45	36	19
9	44	37	18
10	43	38	17
11	42	39	16
12	41	40	15
13	40	41	14
14	39	42	13
15	38	43	12
16	37	44	11
17	36	45	10
18	35	46	9
19	34	47	8
20	33	48	7
21	32	49	6
22	31	50	5
23	30	51	4
24	29	52	3
25	28	53	2
26	27	54	1

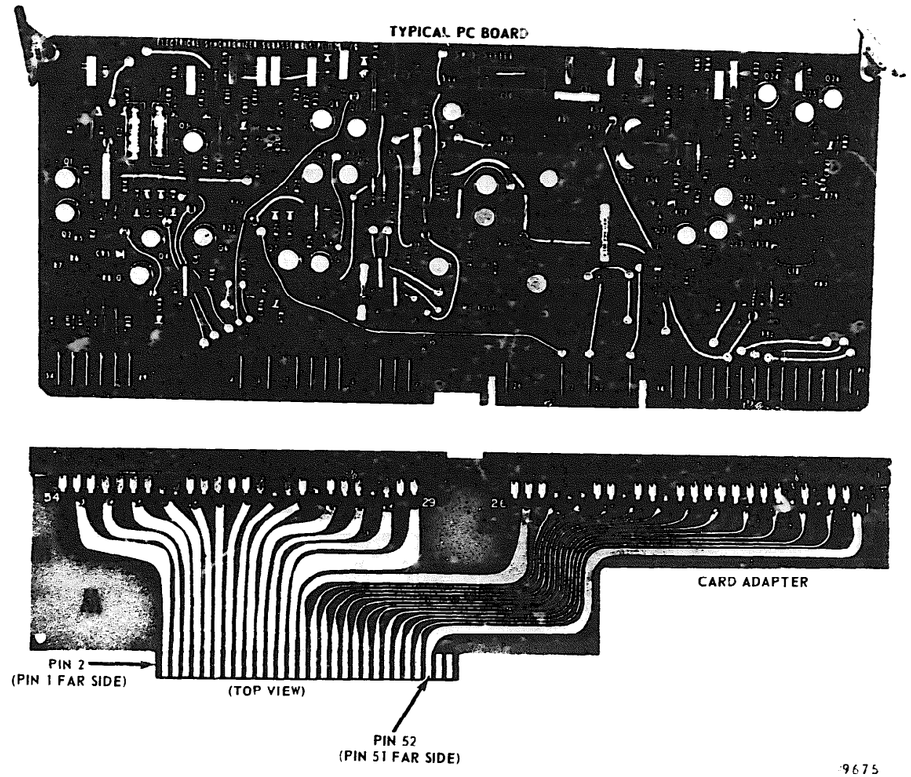


Figure 9. Printed Circuit Card Adapter MX-9092/USM-371 26 Pin SN-394 (Black)

Table 6. Printed Circuit Card Adapter MX-9093/USM-371
Pin Cross Reference

ADAPTER MX-9093/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9093/USM-371	CARD TESTER PIN NUMBER
A	1	N	12
B	2	P	13
C	3	R	14
D	4	S	15
E	5	T	16
F	6	U	17
H	7	V	18
J	8	W	19
K	9	X	20
L	10	Y	21
M	11	Z	22

#G, I, O, Q - omitted

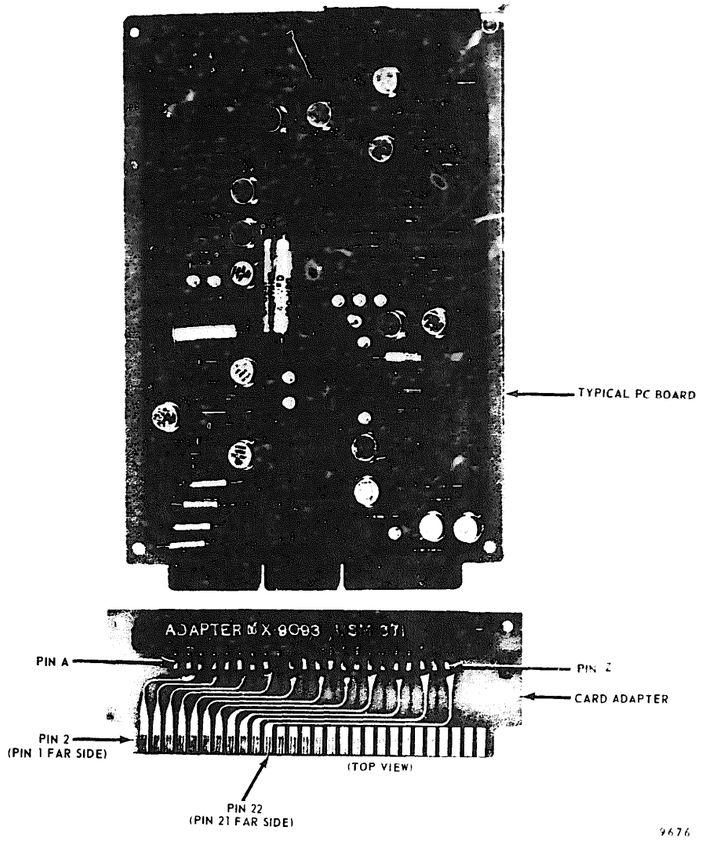


Figure 10. Printed Circuit Card Adapter MX-9093/USM-371
22 Pin MD-674

Table 7. Printed Circuit Card Adapter MX-9094/USM-371 Pin Cross Reference

ADAPTER MX-9094/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9094/USM-371	CARD TESTER PIN NUMBER
1	1	45	23
3	2	47	24
5	3	49	25
7	4	51	26
9	5	53	27
11	6	55	28
13	7	57	29
15	8	59	30
17	9	61	31
19	10	63	32
21	11	65	33
23	12	67	34
25	13	69	35
27	14	71	36
29	15	73	37
31	16	75	38
33	17	77	39
35	18	79	40
37	19	81	41
39	20	83	42
41	21	85	43
43	22		

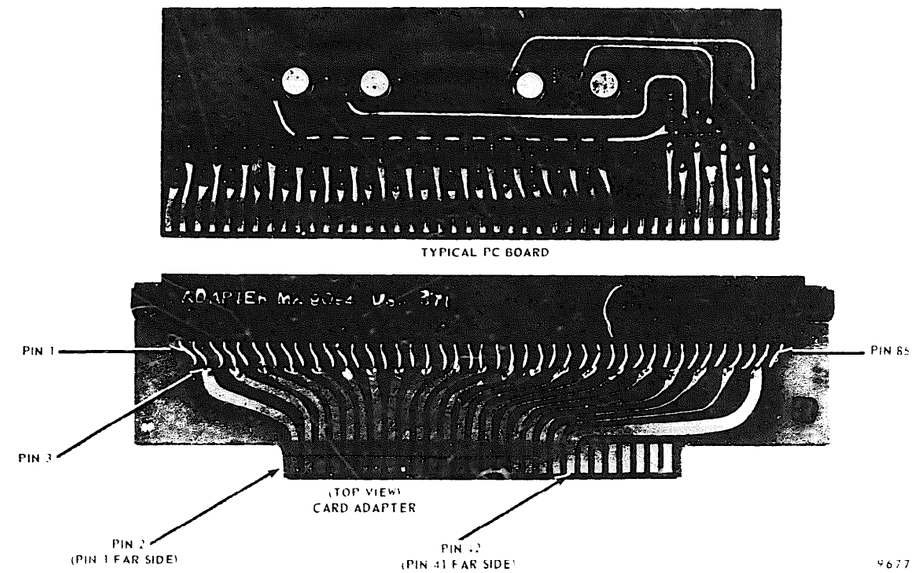


Figure 11, Printed Circuit Card Adapter MX-9094/USM-371 43/86 Pin FGC

Table 8. Printed Circuit Card Adapter MX-9095/USM-371 Pin Cross Reference

ADAPTER MX-9095/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9095/USM-371	CARD TESTER PIN NUMBER
1	56	31	54 (+5V)
2	51	32	No connection
3	No connection	33	55
4	49	34	53
5	47	35	52
6	45	36	50
7	43	37	48
8	41	38	46
9	39	39	44
10	37	40	42
11	35	41	40
12	33	42	38
13	31	43	36
14	29	44	34
15	27	45	32
16	25	46	30
17	23	47	28
18	21	48	26
19	19	49	24
20	17	50	22
21	15	51	20
22	13	52	18
23	11	53	16
24	9	54	14
25	7	55	12
26	5	56	10
27	3	57	8
28	No connection	58	6
29	No connection	59	4
30	1	60	2

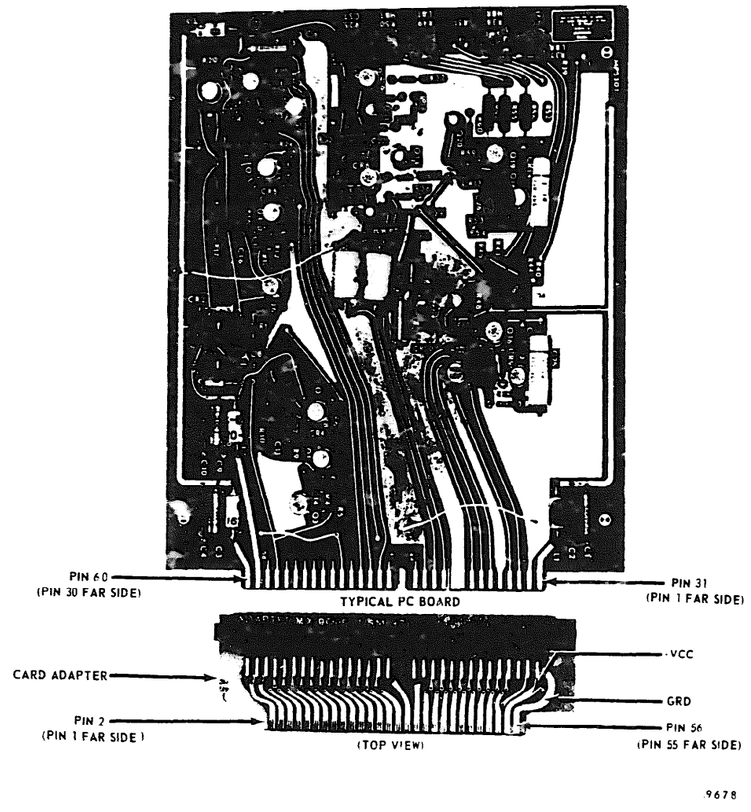


Figure 12. Printed Circuit Card Adapter MX-9095/USM-371 60 Pin TCU

Table 9. Printed Circuit Card Adapter MX-9096/USM-371
Pin Cross Reference

ADAPTER MX-9096/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9096/USM-371	CARD TESTER PIN NUMBER
*1	55	A	56 (GRD.)
*2	53	B	54 (+4.75V)
3	51	C	52
4	49	D	50
5	47	E	48
6	45	F	46
7	43	H	44
8	41	J	42
9	39	K	40
10	37	L	38
11	35	M	36
12	33	N	34
13	31	P	32
14	29	R	30
15	27	S	28
16	25	T	26
17	23	U	24
18	21	V	22
19	19	W	20
20	17	X	18
21	15	Y	16
22	13	Z	14
23	11	AA	12

* If these pins are Power/GRD they are tied to +4.5V/GRD on Autodin Card itself.

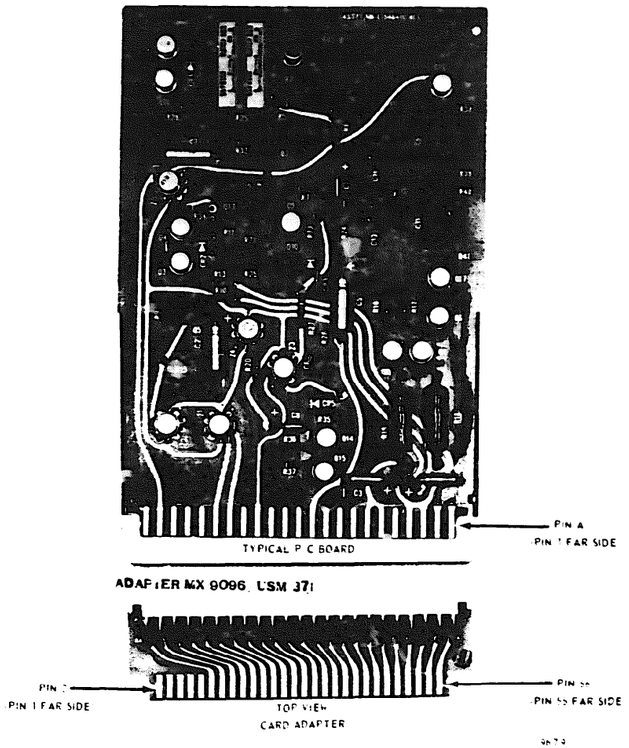


Figure 13. Printed Circuit Card Adapter MX-9096/USM-371
46 Pin GDE

Table 10. Printed Circuit Card Adapter MX-9097/USM-371
Pin Cross Reference

ADAPTER MX-9097/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9097/USM-371	CARD TESTER PIN NUMBER
1	25	13	13
2	24	14	12
3	23	15	11
4	22	16	10
5	21	17	9
6	20	18	8
7	19	19	7
8	18	20	6
9	17	21	5
10	16	22	4
11	15	23	3
12	14	24	2
		25	1

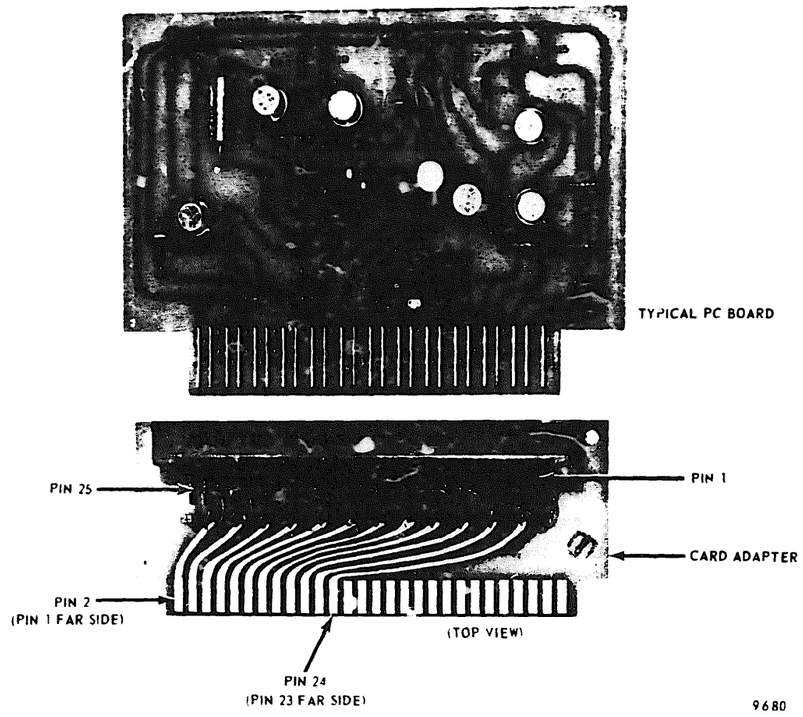
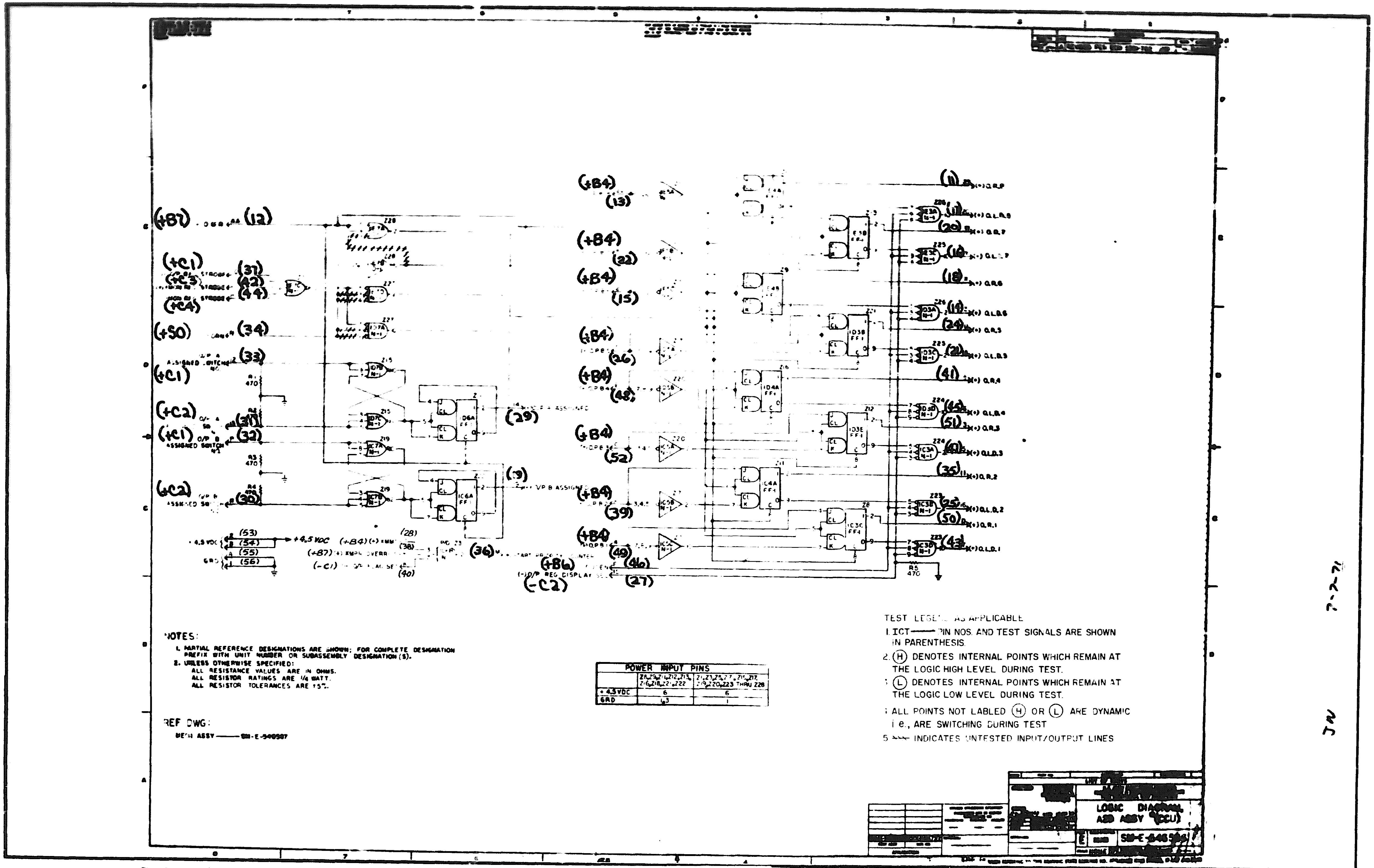
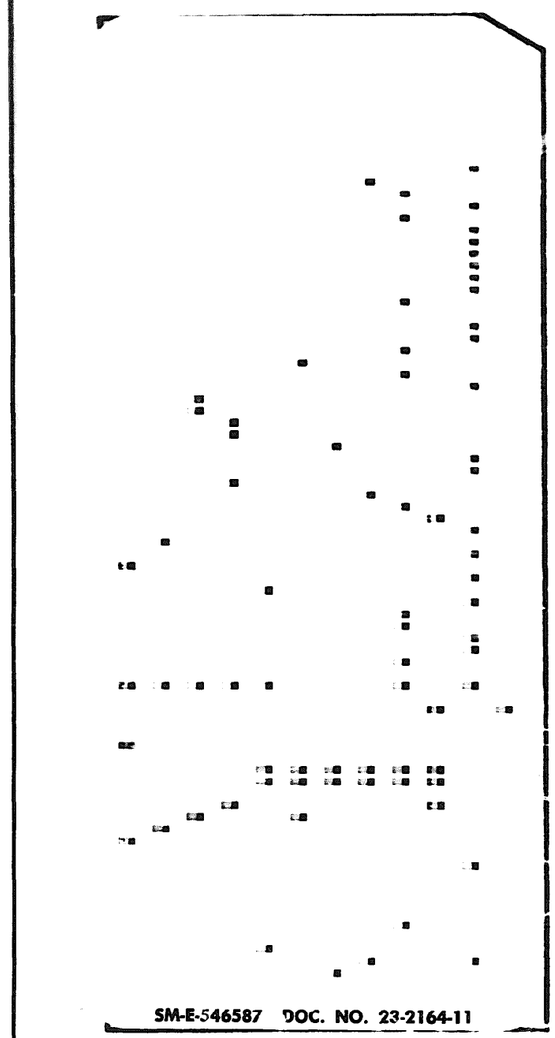


Figure 14. Printed Circuit Card Adapter MX-9097/USM-371
25 Pin FGC

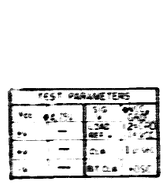


P.C. Assembly SM-E-546587

 P. C. Logic: SM-E-54686 Doc. No. 23- 2164-11



SM-E-546587 DOC. NO. 23-2164-11



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

COVT APPD. JN DATE 2-2-71

TEST LEGEND AS APPLICABLE

1 ICT —— Pin NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST

5 ⋙ INDICATES UNTESTED INPUT/OUTPUT LINES

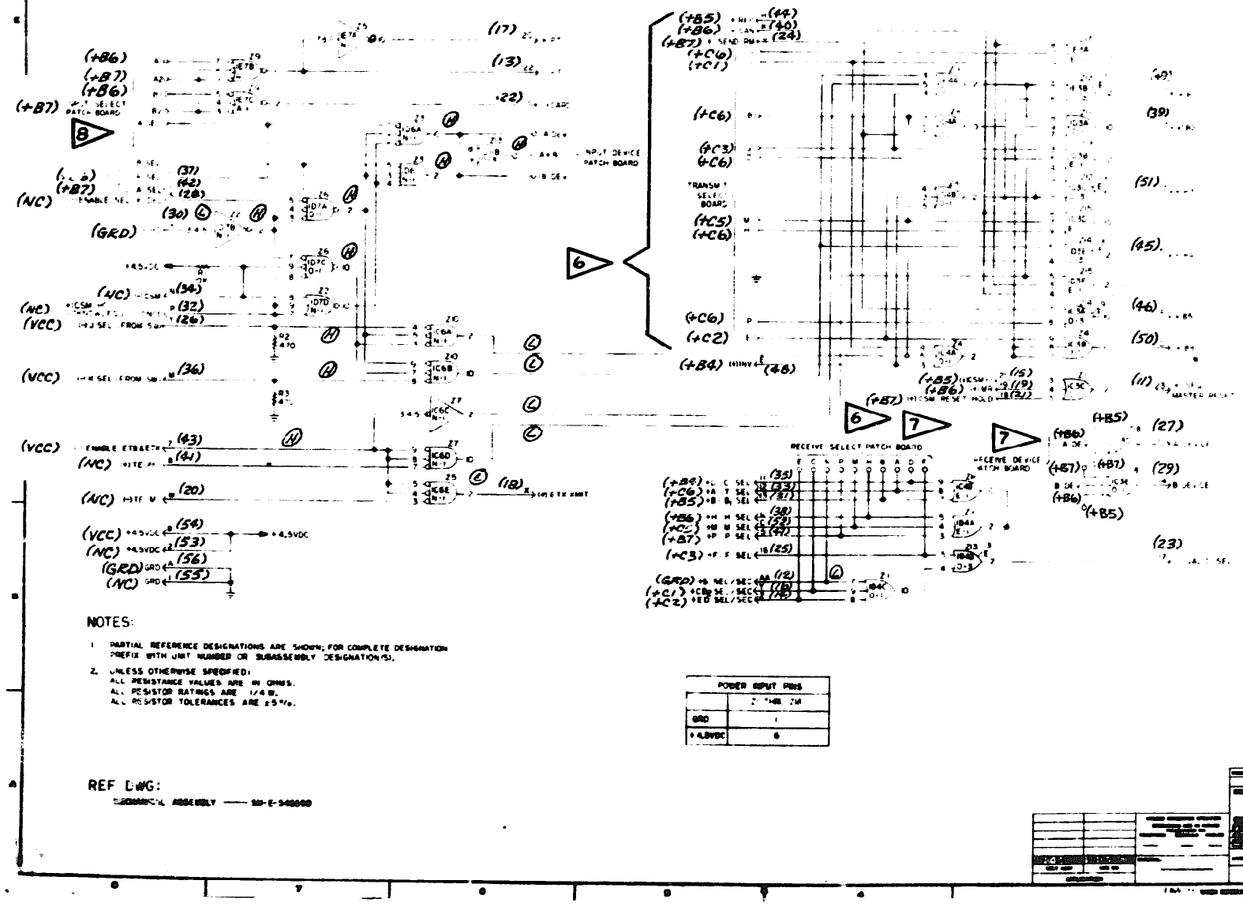
5 PATCH SIGNALS FROM RECEIVE SELECT PATCH BOARD TO TRANSMIT SELECT PATCH BOARD. REFER TO INSTRUCTIONS ON WAVEFORM SHEET.

7 PATCH SIGNALS FROM RECEIVE SELECT PATCH BOARD TO TO RECEIVE DEVICE PATCH BOARD. REFER TO INSTRUCTIONS ON WAVEFORM SHEET.

8 PATCH INPUT SELECT PATCH BOARD IN ACCORDANCE WITH INSTRUCTIONS ON WAVEFORM SHEET.

9. PINS 26, 36 AND 43 CONNECTED TO VCC THROUGH 510 OHM RESISTORS.

10. PINS 12 AND 30 CONNECTED TO GRD THROUGH 3K OHM RESISTORS.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR RATINGS ARE 1/4 W.
   ALL RESISTOR TOLERANCES ARE ±5%.

POWER INPUT PINS	
GRD	1
+4.5VDC	6

REF DWG:
ASSEMBLY —— SM-E-546589

LOGIC DIAGRAM, ASSY A61 (CCU)
SM-E-546589

2-2-71

SM-E-546590 DOC. NO. 23-2165-12

GOVT APPD. JN DATE 7-7-71

TEST PARAMETERS

Vcc	+4.75	SIG V	VCC
2V		LOADS REF V	1/2 VCC 1/2 VRD
+V		CLK	1 μ SEC
-V		BIT CLK	+OSC

ROW ASSIGNMENT

10	+B4
1	+B5
2	+B6
3	+B7
4	-
5	+C5
6	+C6
7	+C1
8	+C2
9	+C3

INPUT PINS	COL	SIG
	63	+C0
16	64	-C1
16	65	-C2
25	66	-C3
	67	-C4
52	68	+C5
33	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
35, 48	74	+B4
15, 31, 44	75	+B5
19, 37, 38, 40	76	+B6
21, 24, 42, 47	77	+B7
	78	+S0
	79	+S1
	80	+S2
OUTPUT PINS (TEST POINTS)	SWITCH SETTINGS	+C0 REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTINGS
23	A 1 2 3 4 5 6 7 / B 7 4 6 8 10 5 #
89	A 1 2 3 4 5 6 7 / B 7 4 6 8 10 5 10
39	A 1 2 3 4 5 6 7 8 9 / B 2 3 7 4 6 5 9 1 11
91	A 1 2 3 4 5 6 / B 7 8 10 5 1 3
85	A 1 2 3 4 5 6 7 8 9 / B 2 9 2 NT NT NT NT 6 6
86	A 1 2 3 4 5 / B 2 3 7 11 #
90	A 1 2 3 4 5 6 7 / B 2 4 6 8 10 1 11
11, 27, 30	A 1 2 3 / B 11 #
14, 17, 22	A 1 2 3 / B 1 #

FROM PATCH BOARD	TERMINAL	TO PATCH BOARD	TERMINAL
RCV. SEL.	A	TX. SEL.	A,B,C,F,P
RCV. SEL.	C	TX. SEL.	C
RCV. SEL.	F	TX. SEL.	E
RCV. SEL.	E	TX. SEL.	G
RCV. SEL.	M	TX. SEL.	M
RCV. SEL.	3	RCV. DEV.	A(Z1%-3)
RCV. SEL.	9	RCV. DEV.	B(Z1%-9)
RCV. SEL.	4	RCV. DEV.	A(Z1%-4)
RCV. SEL.	8	RCV. DEV.	B(Z1%-8)
RCV. SEL.	F	RCV. DEV.	A(Z1%-6)
RCV. SEL.	P	RCV. DEV.	B(Z1%-7)
INPUT SEL.	A	INPUT SEL.	A1,B1
INPUT SEL.	B	INPUT SEL.	A2,B2

DYNATRONICS TESTAGRAM

WAVEFORMS — 4 μ SEC

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

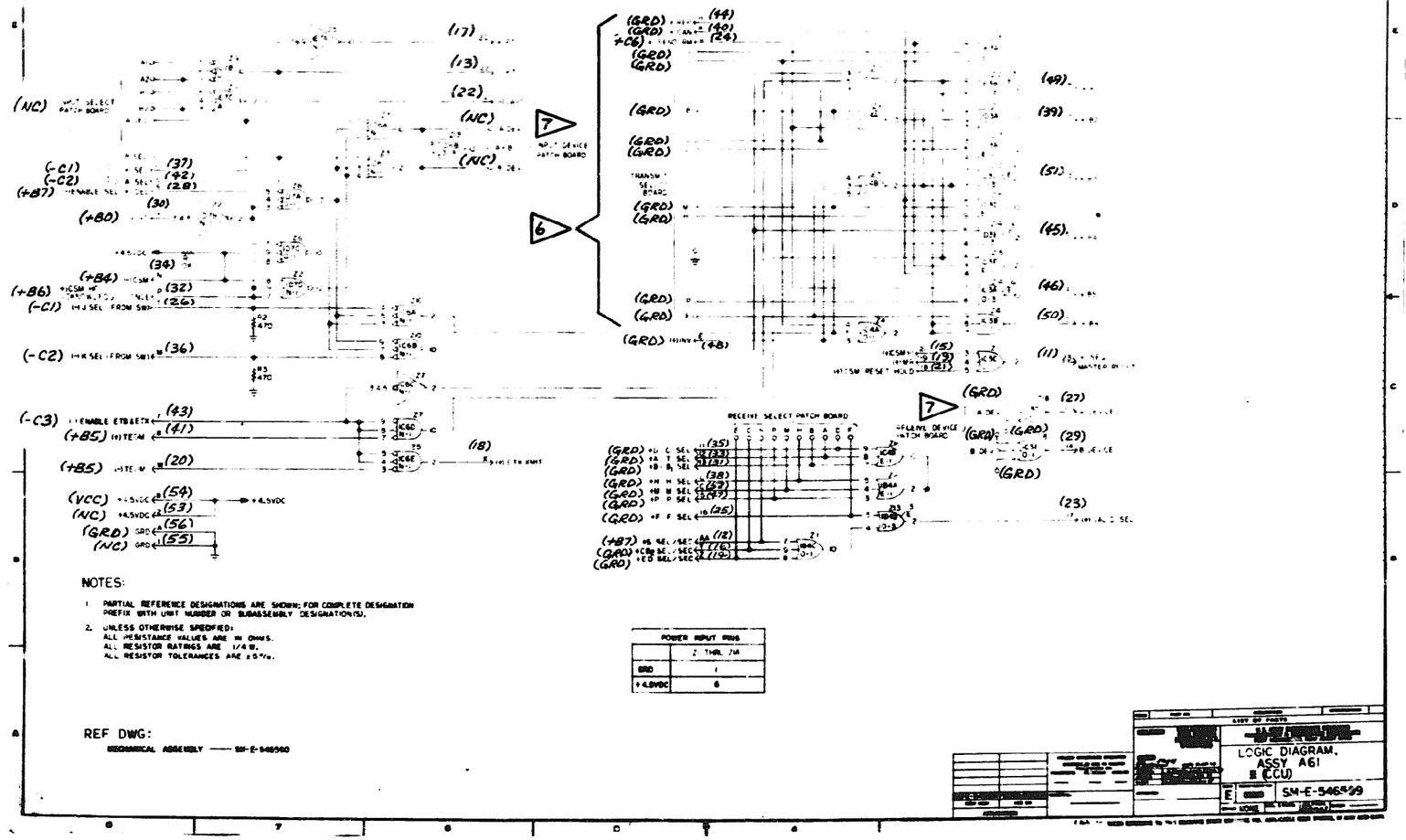
   IN ICT-103 TESTER PRESS"B" SWITCH "#" WHERE INDICATED BY "#": VALID TEST IS GO INDICATION.
4. BEFORE PROCEEDING WITH TEST, INSTALL JUMPERS ON CARD IN ACCORDANCE WITH INSTRUCTIONS IN TABLE AT THE BOTTOM OF THE WAVEFORM CHART.
5. NT INDICATES NO TEST.

TEST LEGEND AS APPLICABLE

1. ICT ——— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ⩙ INDICATES UNTESTED INPUT/OUTPUT LINES

6 PATCH ALL TRANSMIT SELECT TERMINALS TO GRD TERMINALS.

7 PATCH INPUT DEVICE A+B TERMINAL TO RECEIVE DEVICE A DEV TERMINAL AND B DEV TERMINAL. PATCH THE REMAINING 4 TERMINALS OF A DEV + B DEV TO GRD TERMINALS.



NOTES:

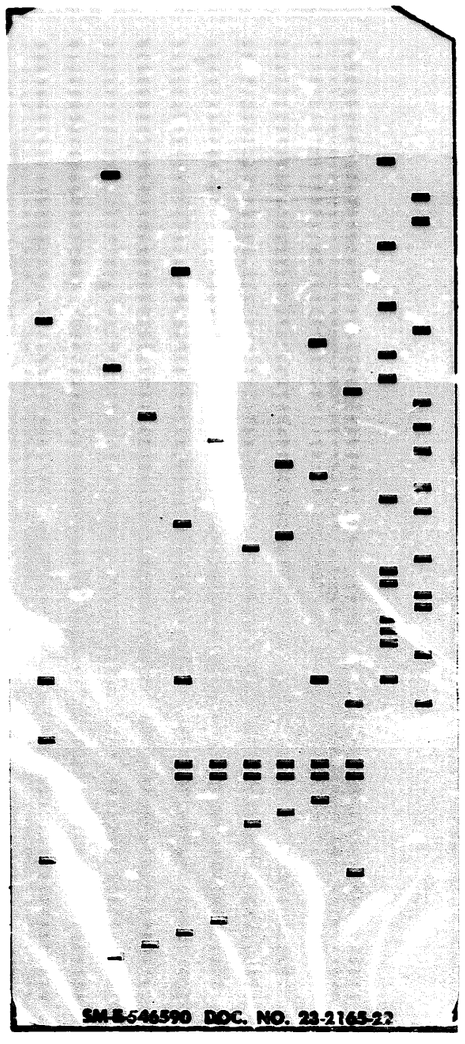
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR RATINGS ARE 1/4 W.
   ALL RESISTOR TOLERANCES ARE ±5%.

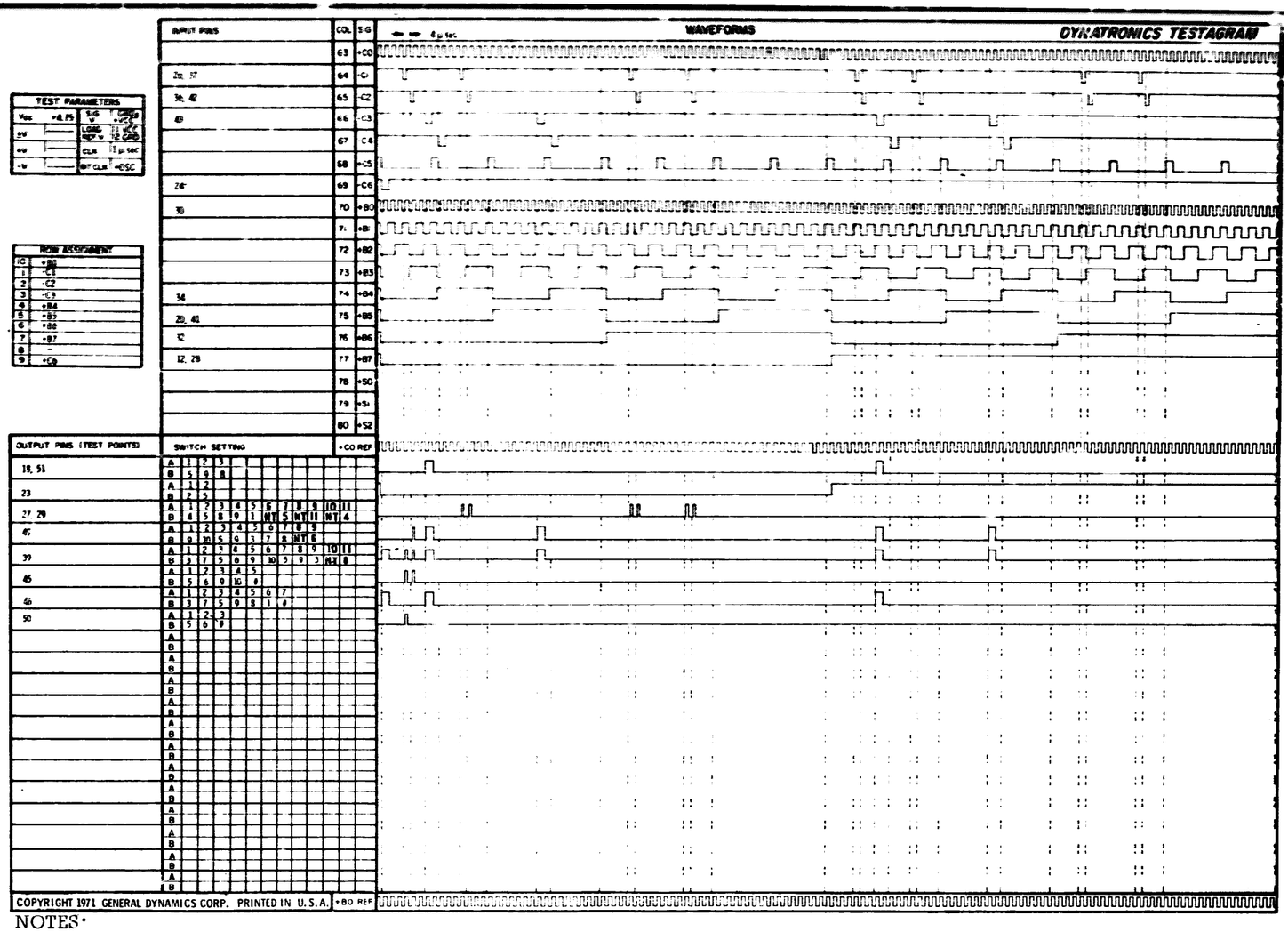
REF DWG:
MECHANICAL ASSEMBLY —— SM-E-546590

POWER INPUT PINS	
	2 THRU 7/8
GRD	1
+4.5VDC	9

LOGIC DIAGRAM, ASSY A61 (CCU)
SM-E-546589

P.C. Assembly SM-E-546590
P.C. Logic SM-E-546589



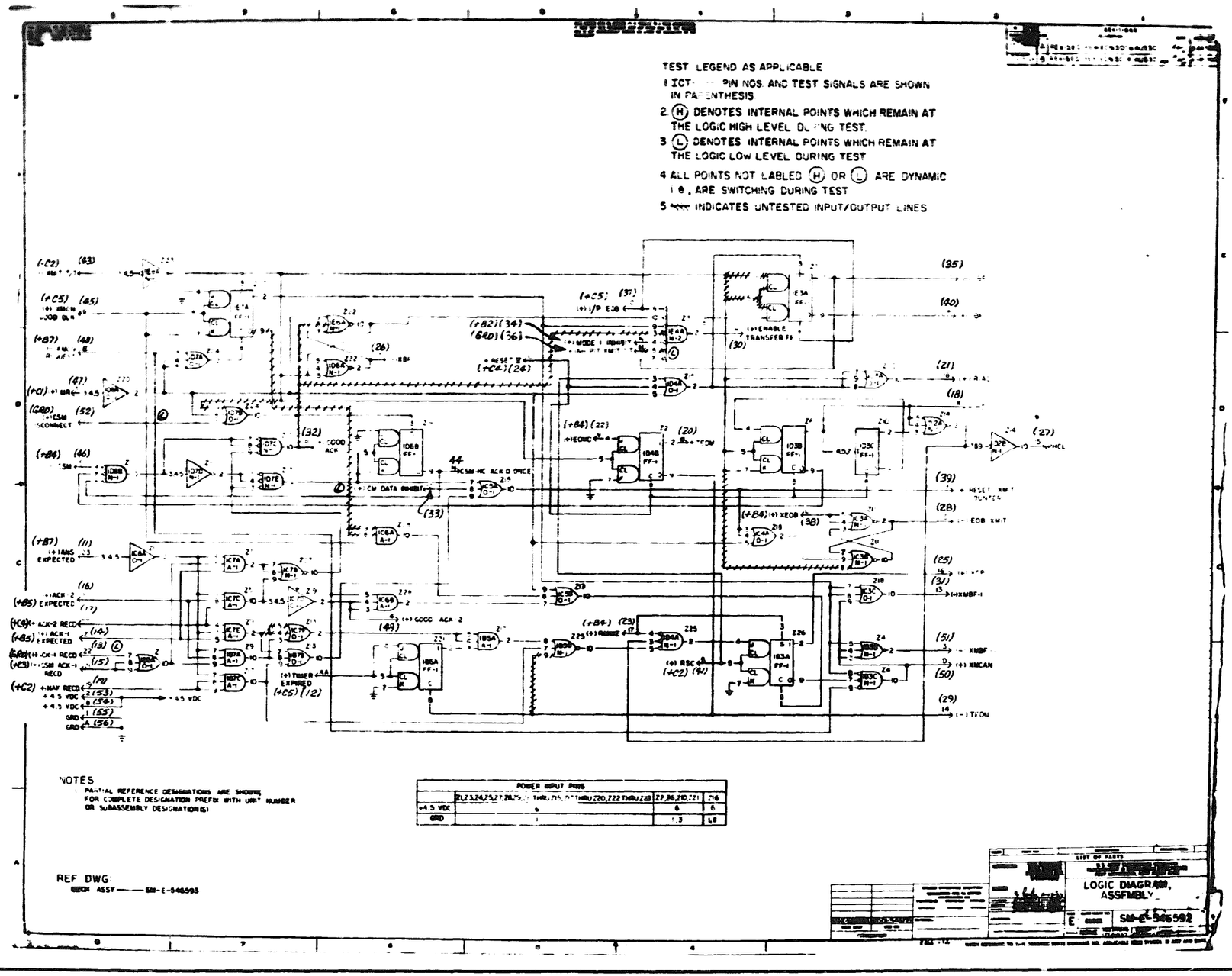


NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO 4.75V.
3. IN ICT-102 "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

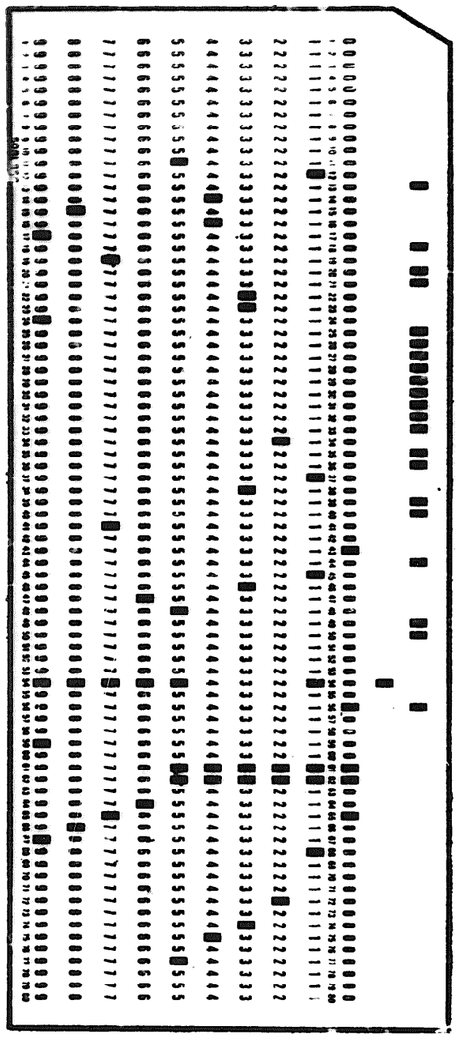
   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" : VALID TEST IS GO INDICATION.
4. BEFORE PRECEEDING WITH TEST PATCH ALL TRANSMIT SELECT PATCH BOARD TERMINALS TO GRD.
5. PATCH INPUT DEVICE A +B TERMINAL TO RECEIVE DEVICE A DEV AND B DEV TERMINALS PATCH REMAINING 4 TERMINALS OF RECEIVE DEVICE PATCH BOARD TO GRD.
6. NT INDICATES NO TEST.

GOVT APPD. JN DATE 7-7-71



P.C. Assembly SM-E-546593

P.C. Logic SM-E-546592

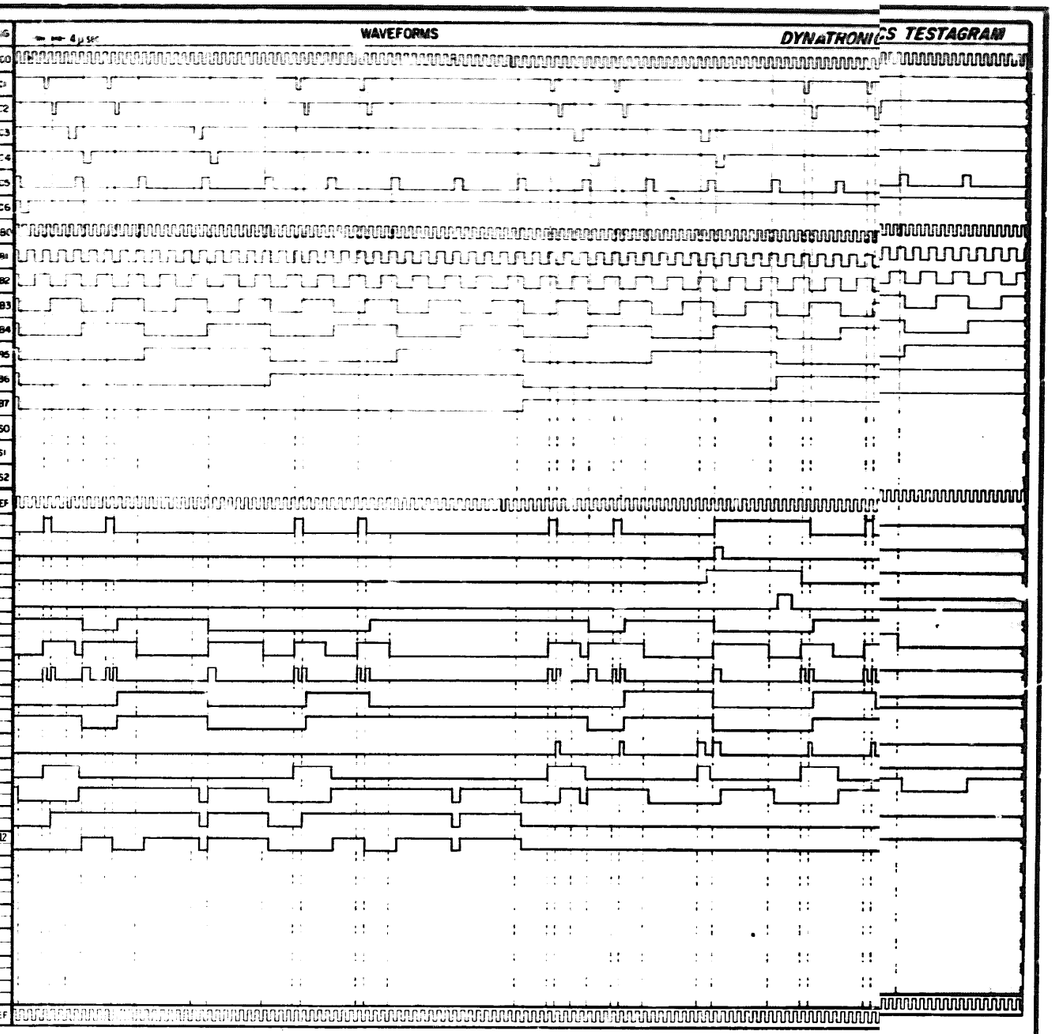


TEST PARAMETERS			
+5VEXT	+4.75V	SIG V	SIG GND
+5V	—	LOAD REF V	12 TRI 11-VCC
+4V	—	CLK	1 μSEC
-5V	—	BIT CLR	+OSC

ROW ASSIGNMENT	
10	-C2
1	+C5
2	+B2
3	+B4
4	+B5
5	+B7
6	+C1
7	+C2
8	+C3
9	+C4

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
26	A 1 2 3 4 / B 6 4 8 3 7
32, 19	A 1 2 3 / B 5 7 #
44	A 1 2 3 / B 10 3 #
30	A 1 2 3 / B 2 9 #
20, 29*	A 1 2 3 4 / B 2 9 11 5
35, 40*	A 1 2 3 4 / B 6 4 9 2 8
21	A 1 2 3 4 5 6 / B 4 6 8 10 2 6
18	A 1 2 3 4 / B 9 11 6 5
27	A 1 2 3 4 / B 2 1 11 6
39	A 1 2 3 4 5 6 7 5 9 10 / B 11 2 10 1 6 10 3 7 7 9
28	A 1 2 3 4 5 6 7 8 / B 4 1 11 8 7 4 6 2
25	A 1 2 3 4 5 6 7 8 9 10 / B 2 1 7 11 9 8 3 7 5 #
31, 51*	A 1 2 3 4 5 6 7 - 9 / B 8 7 11 9 4 3 7 5 #
50	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 2 7 1 7 11 9 9 3 8 3 7 5

INPUT PINS	COL	SIG
	63	+C0
47*	64	+C1
43, 19*, 41*	65	+C2
15*	66	+C3
17*, 24*	67	+C4
45, 12, 37	68	+C5
	69	-C6
	70	+B0
	71	+B1
36	72	+B2
	73	+B3
22, 23, 46, 38	74	+B4
16, 14	75	+B5
	76	+B6
48, 11	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+C0 REF

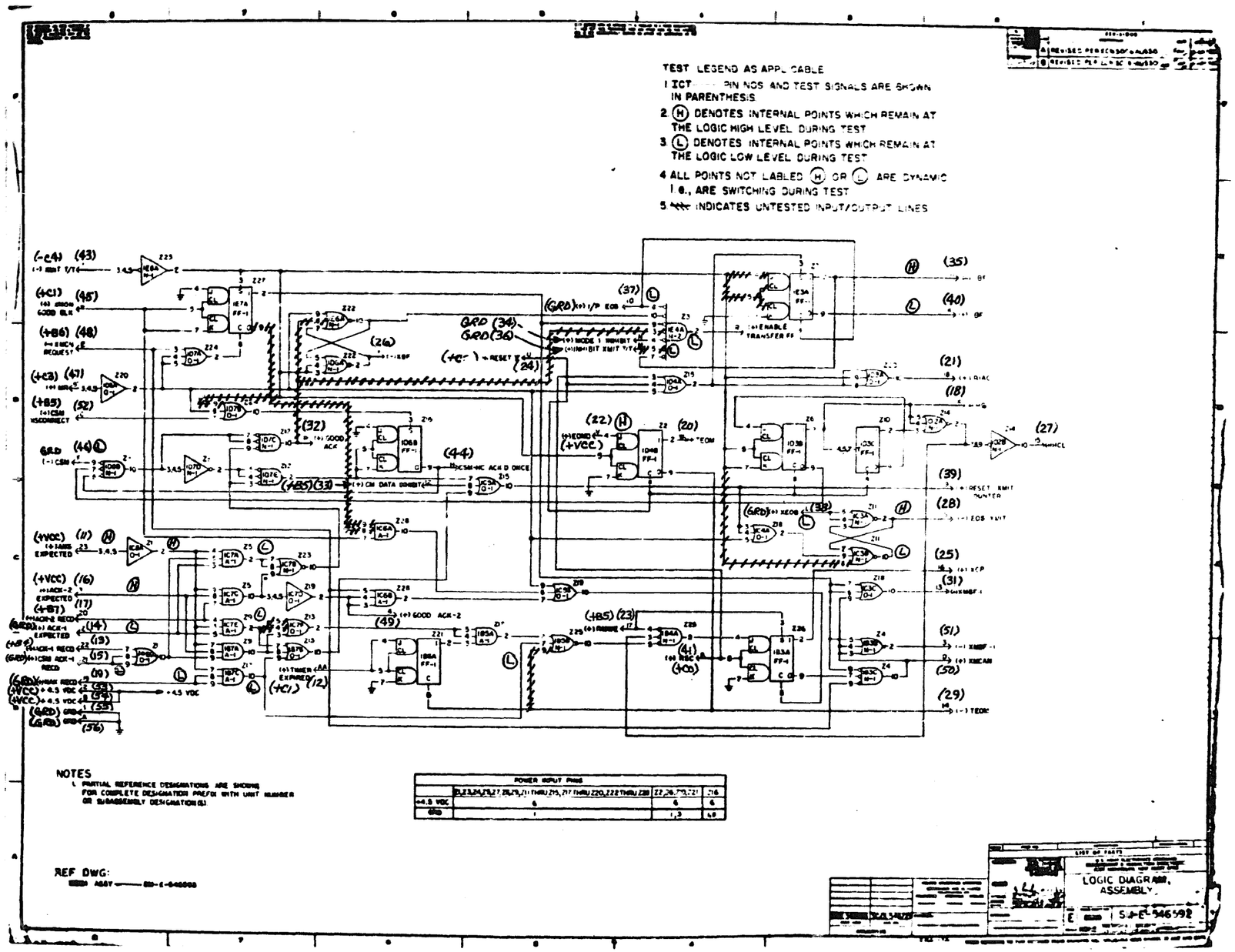


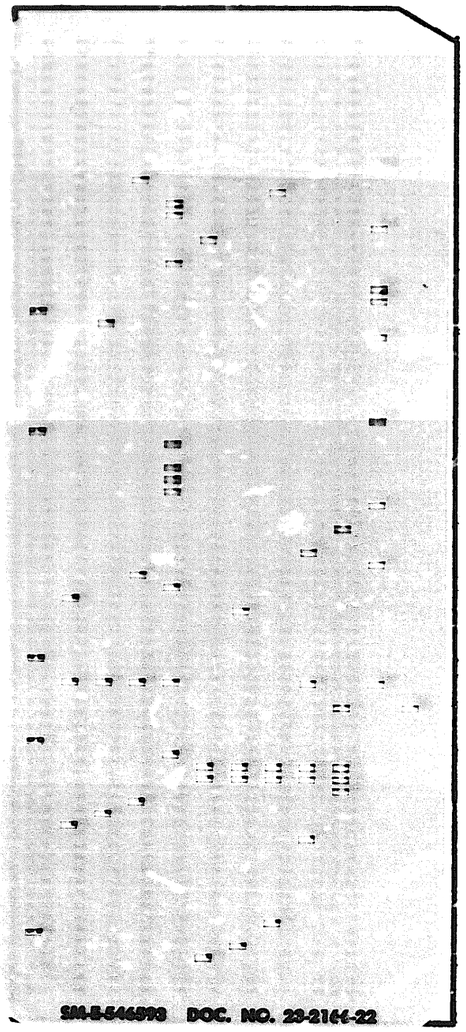
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.

GOVT APPD. JN DATE 7-7-71


TEST LEGEND AS APPLICABLE
1 ICT PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST
5 INDICATES UNTESTED INPUT/OUTPUT LINES
NOTES
1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
REF DWG:
LOGIC DIAGRAM, ASSEMBLY
SM-E-546592



TEST PARAMETERS

ϕV_{CC}	ϕ 4.75V	SIG V	ϕVCC & GRD
+V	—	LOAD REF V	+VCC=GND -VCC=VCC
0V	—	CLK	1 μsec
-V	—	BIT CLR	+05V

ROW ASSIGNMENT

10	+CO
1	-C4
2	+B4
3	+B6
4	+B7
5	GRD
6	+C1
7	+C2
8	+C3
9	+B5

INPUT PINS	COL	SIG
41	63	+CO
45*, 12*	64	-C1
24*	65	+C2
47*	66	-C3
43	67	-C4
	68	+C5
	69	-C6
	70	+BC
	71	+B1
	72	+B2
	73	+B3
13	74	+B4
52, 33, 23	75	+B5
48	76	+B6
17	77	+C7
	78	+SO
	79	+S1
	80	+S2

WAVEFORMS — DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS) — SWITCH SETTING — +CO REF

25
32
44
21
39

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.

GOVT APPD. JN DATE 2-2-71

TEST LEGEND AS APPLICABLE

1 (CT —— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

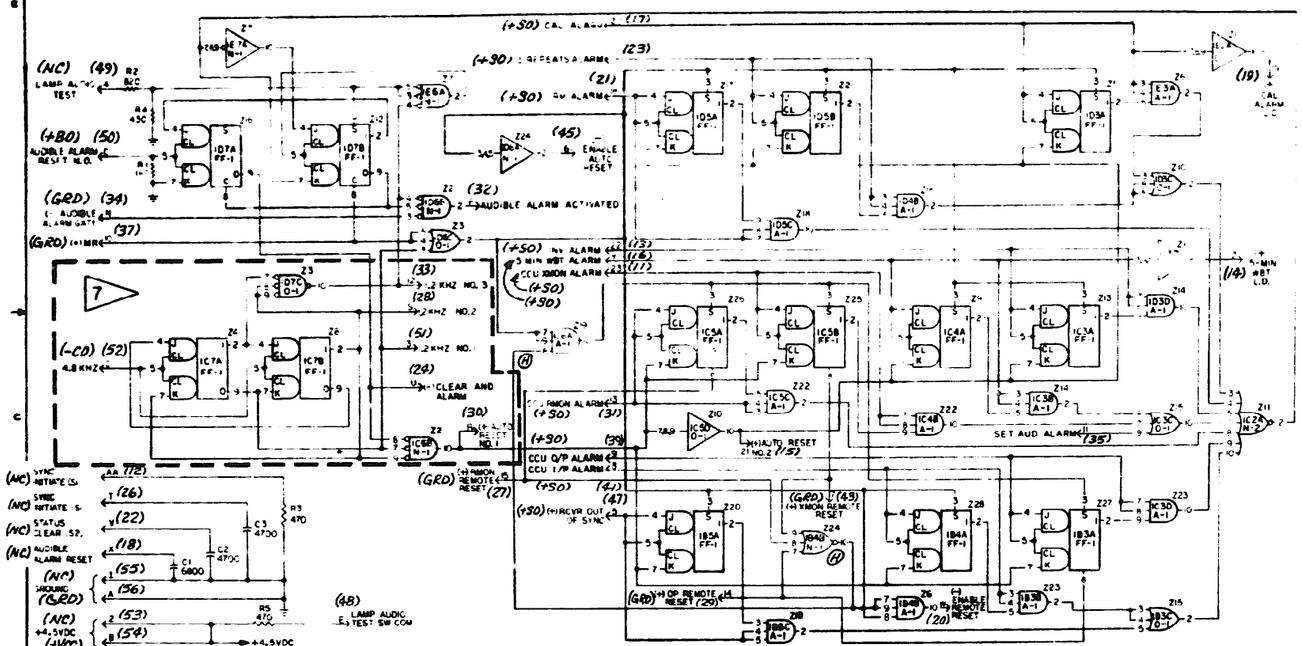
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e. ARE SWITCHING DURING TEST.

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES

6. NC SIGNIFIES "NO CONNECTION".

7 INPUT/OUTPUT LINES IN THIS SECTION ARE TESTED AS AN ASYNCRONOUS COUNTER. ALL OTHER LINES, ALTHOUGH SWITCHING ARE CONSIDERED UNVERIFIED.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR RATINGS ARE 1/4W.
   ALL RESISTOR TOLERANCES ARE ±5%.
   ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS.

REF DWGS:

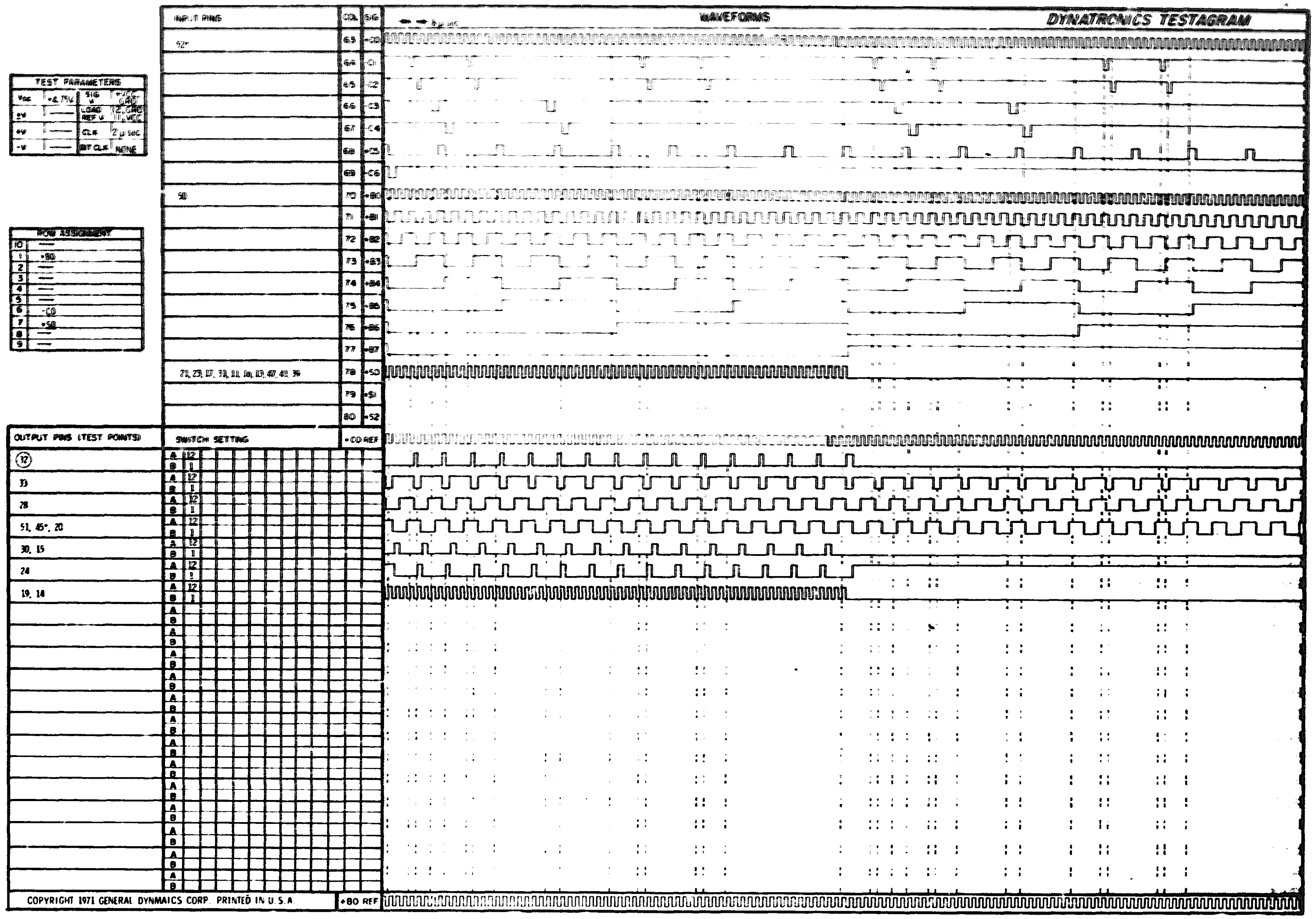
POWER INPUT PINS				
	Z1,Z2,Z3,Z6,Z7,Z10,Z11,Z12, Z14,Z15,Z16,Z19,Z22 THRU Z27,Z29 & Z30	Z4,Z5,Z8,Z13,Z17,Z20,	Z4 & Z8	Z15
GRD	1	14	4,5 & 8	4,5 & 7
+4.5VDC	6	6	6	6

LOGIC DIAGRAM, AUDIBLE ALARM SET & RESET A 22

SM-E-546995

J.W. 7-2-71

.C. Assembly SM-E-546596
.C. Logic SM-E-546595 Doc. No. 2167-11

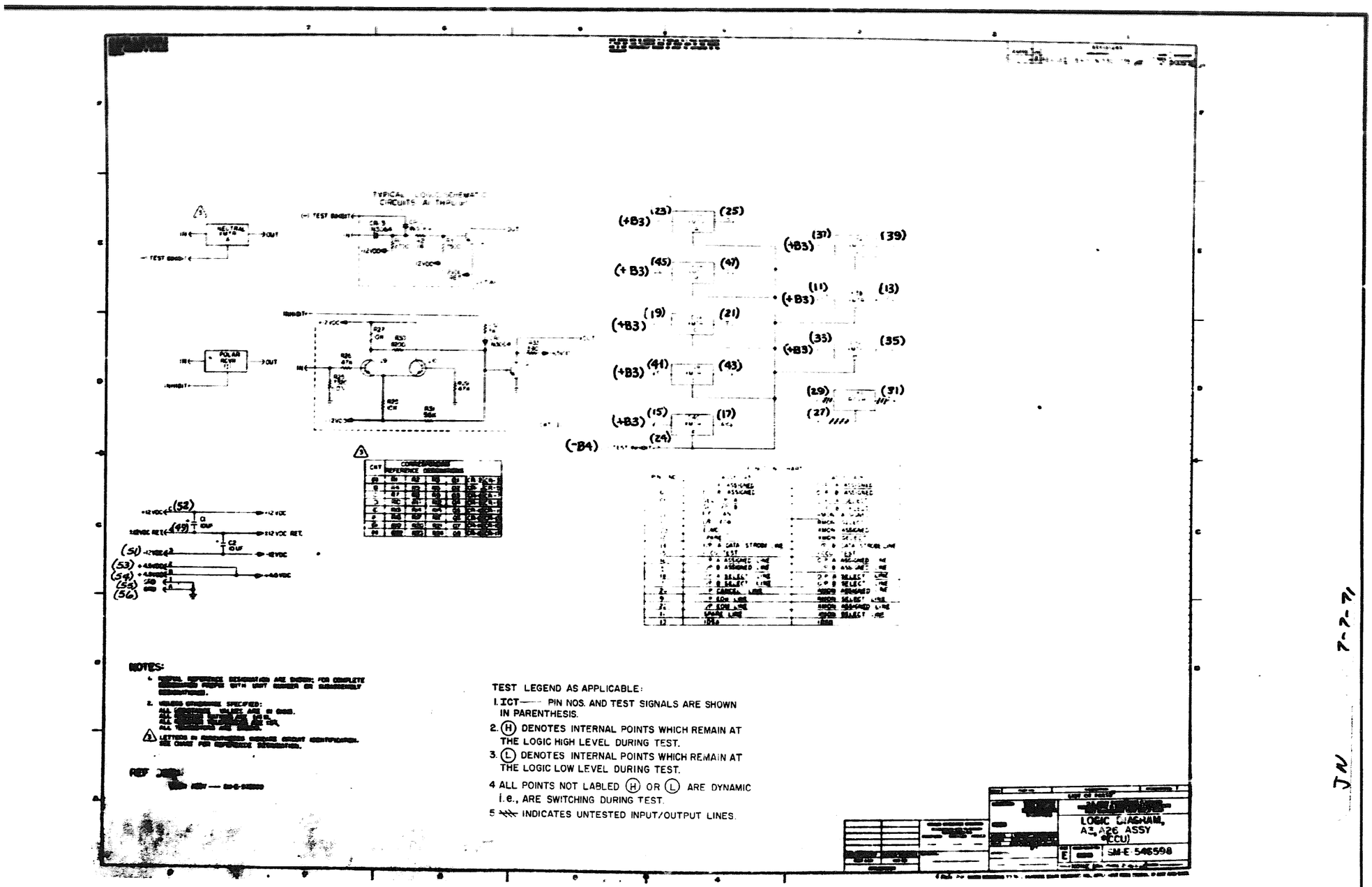


SM-E-546596 DOC. NO. 23-2167-11

NOTES:

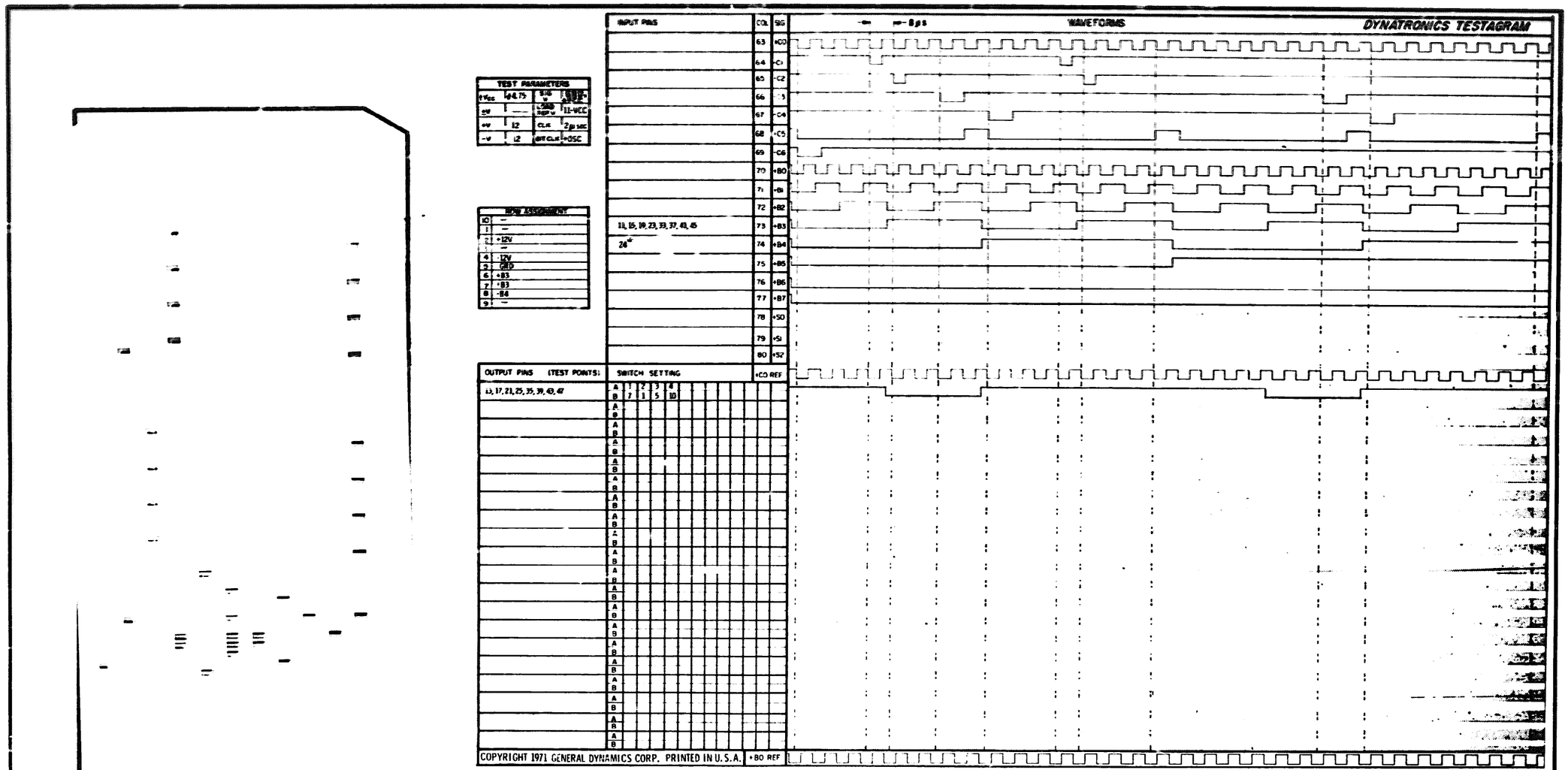
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. OUTPUT SIGNALS ARE NOT SYNCRONOUS WITH TEST SIGNALS BUT ARE SHOWN CORRECTLY WITH RESPECT TO ONE ANOTHER.

GOVT APPD. JN DATE 7-7-71



P.C. Assembly SM-E-546599

P.C. Logic SM-E-546598 Doc. No. 23-2168-11

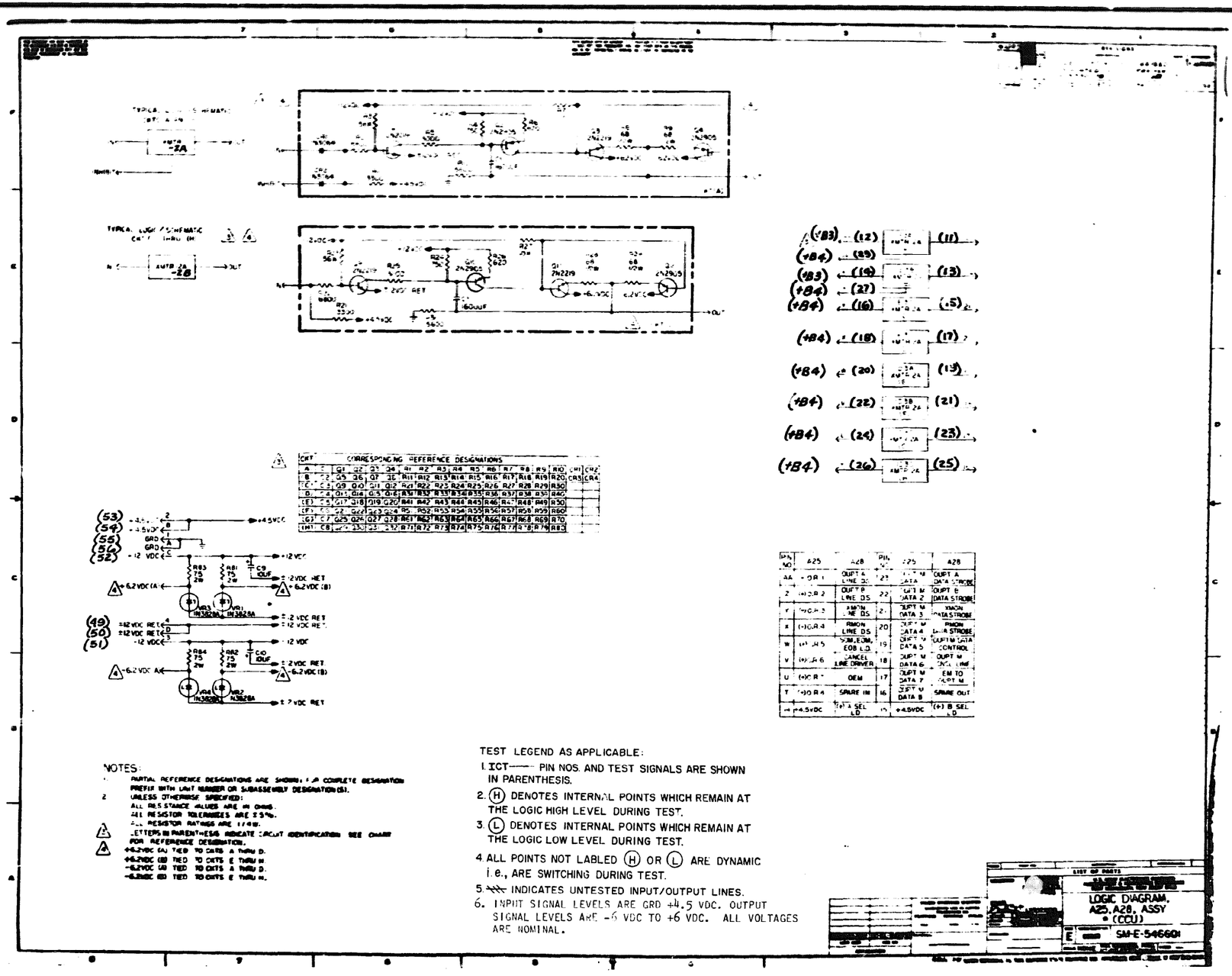


SM-E-546599 DOC. NO. 23-2168-11

NOTES:

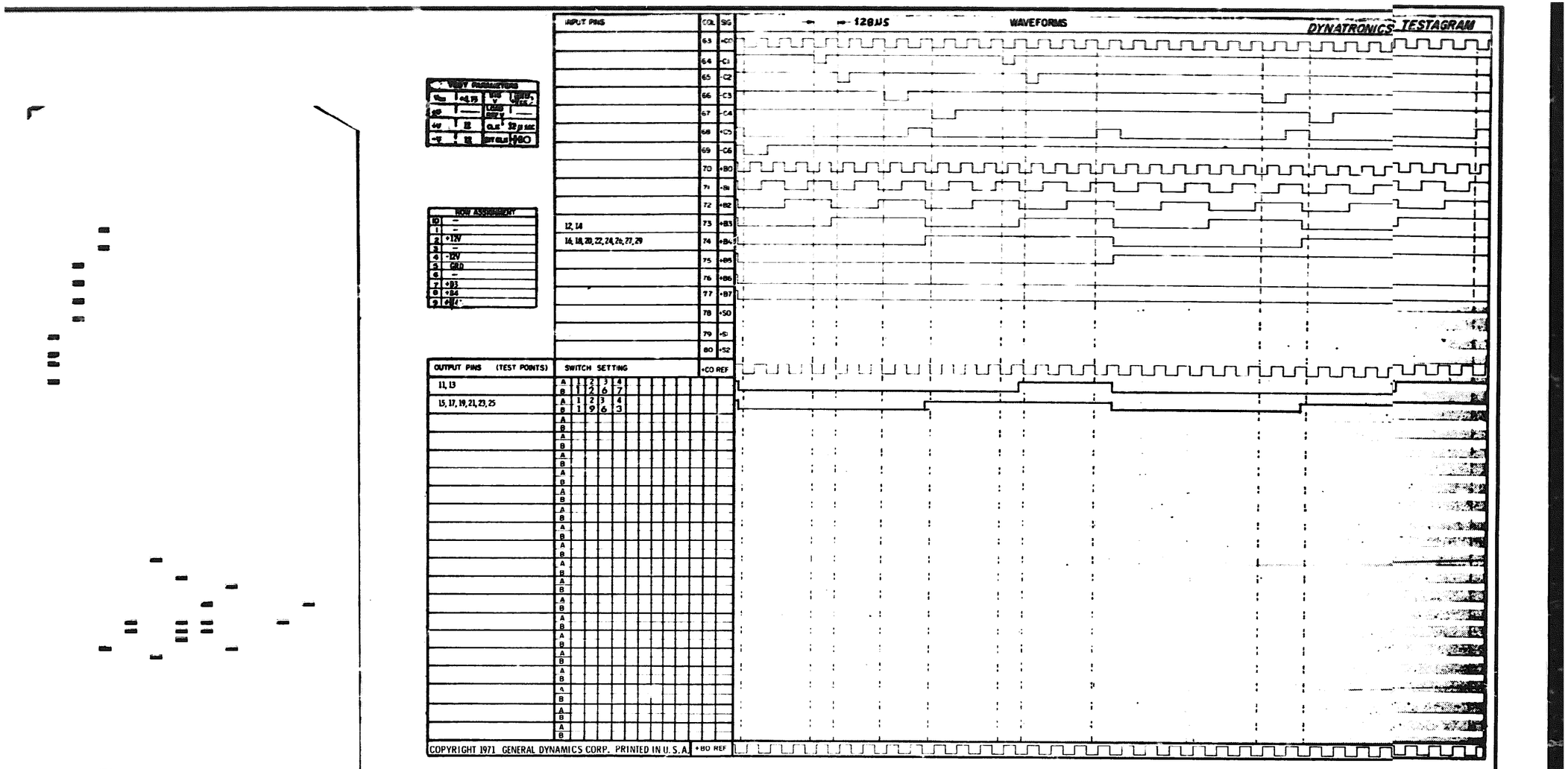
1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

GOVT APPD. JN DATE 7-7-71



P.C. Assembly SM-E-546602

P.C. Logic SM-E-546601 Doc. No. 23- 2169-11

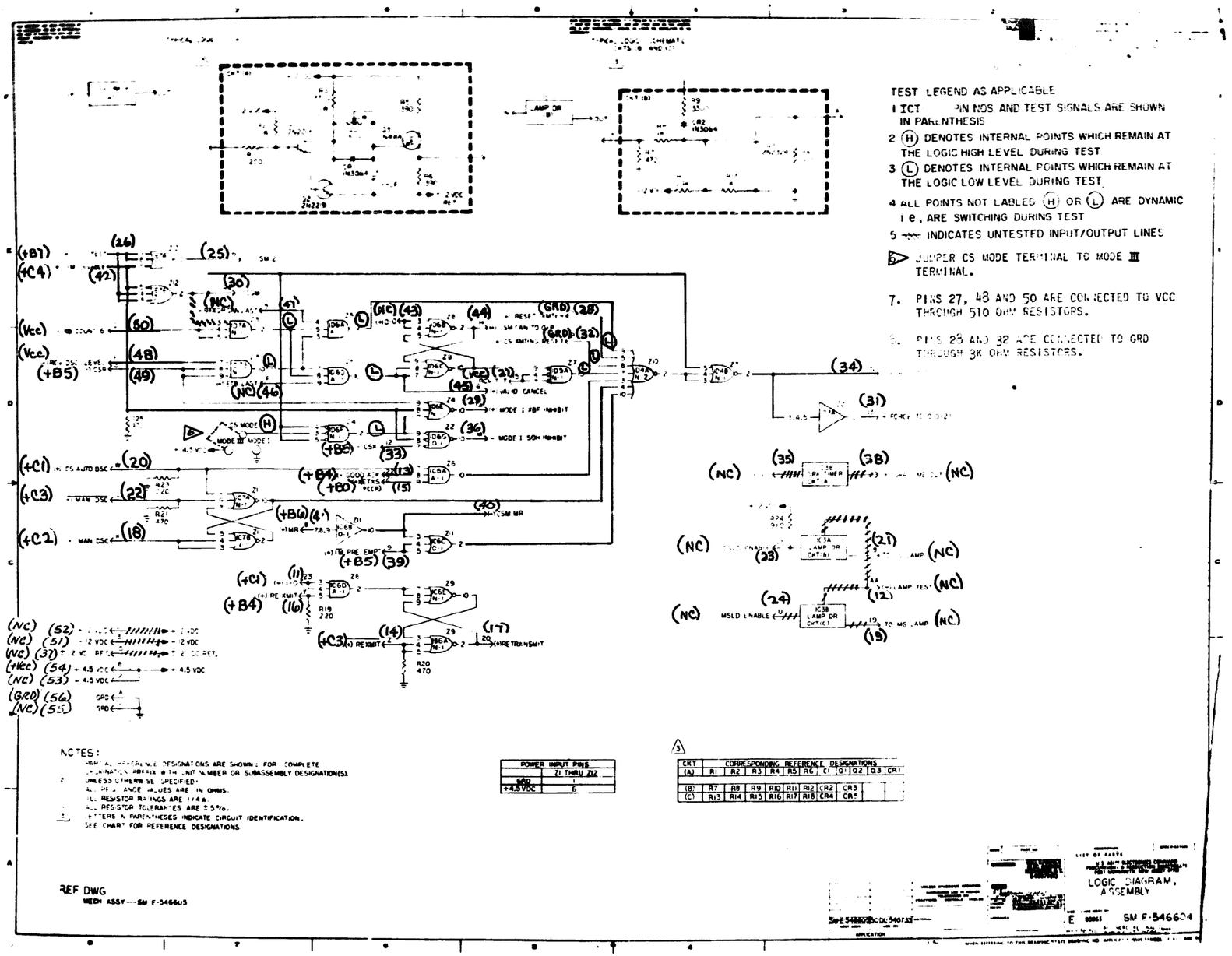


NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. OUTPUT SIGNAL LEVELS ARE +6VDC TO -6VDC.

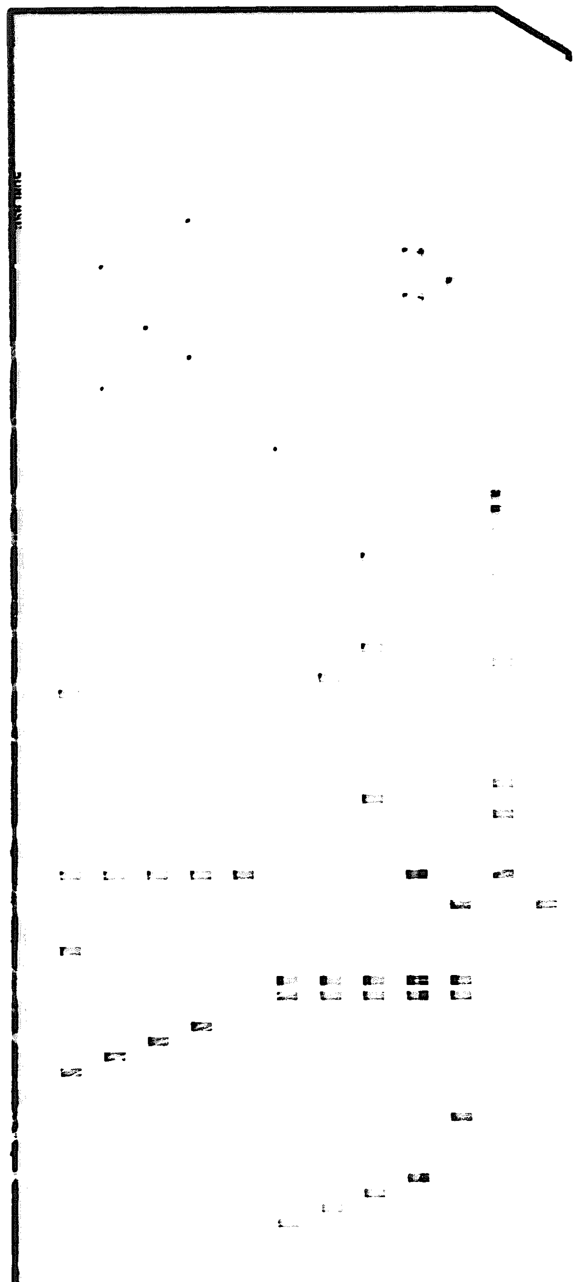
SM-E-546602 DOC. NO. 23-2169-11

GOVT APPD. JN DATE 7-9-71



P.C. Assembly SM-E-546605-001
P.C. Logic SM-E-546604

Doc. No. 23- 2193-12


SM-E-546605 DOC. NO. 23-2193-12

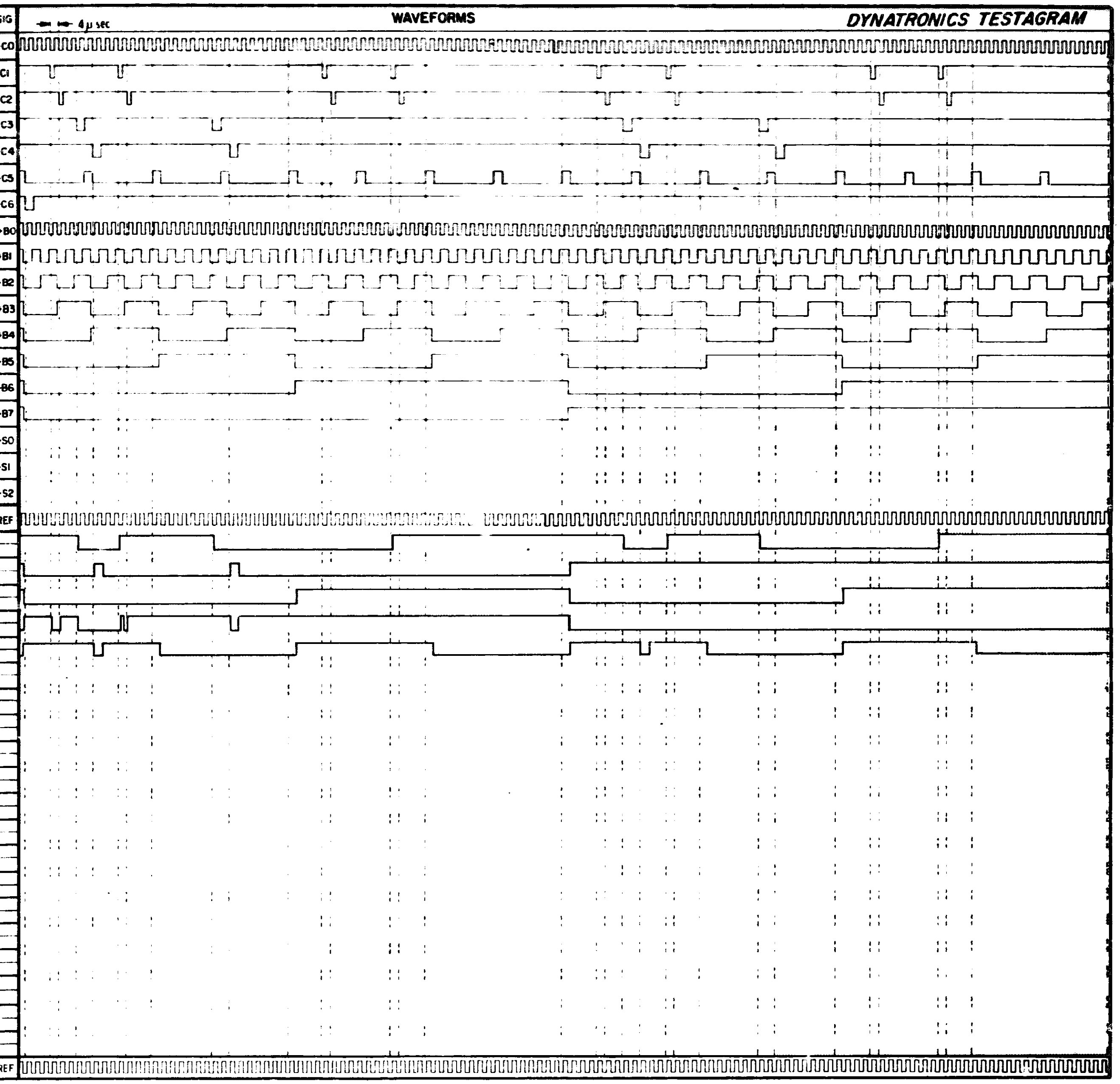
GOVT APPD. JN DATE 7-7-71

TEST PARAMETERS			
Vcc	+4.75	SIG V	GND, +VCC
±V	—	LOAD REF V	11, VCC 12, GND
+V	—	CLK	1 μ sec
-V	—	BIT CLK	+OSC

ROW ASSIGNMENT	
10	+B0
1	+B4
2	+B5
3	+B6
4	+B7
5	—
6	+C1
7	+C2
8	+C3
9	+C4

INPUT PINS	COL	SIG
	63	+C0
11*, 20*	64	-C1
18*	65	-C2
14*, 22*	66	-C3
42*	67	-C4
	68	+C5
	69	-C6
15	70	+B0
	71	+B1
	72	+B2
	73	+B3
13, 16	74	+B4
39, 33, 49	75	+B5
41	76	+B6
26	77	+B7
	78	+S0
	79	+S1
	80	+S2

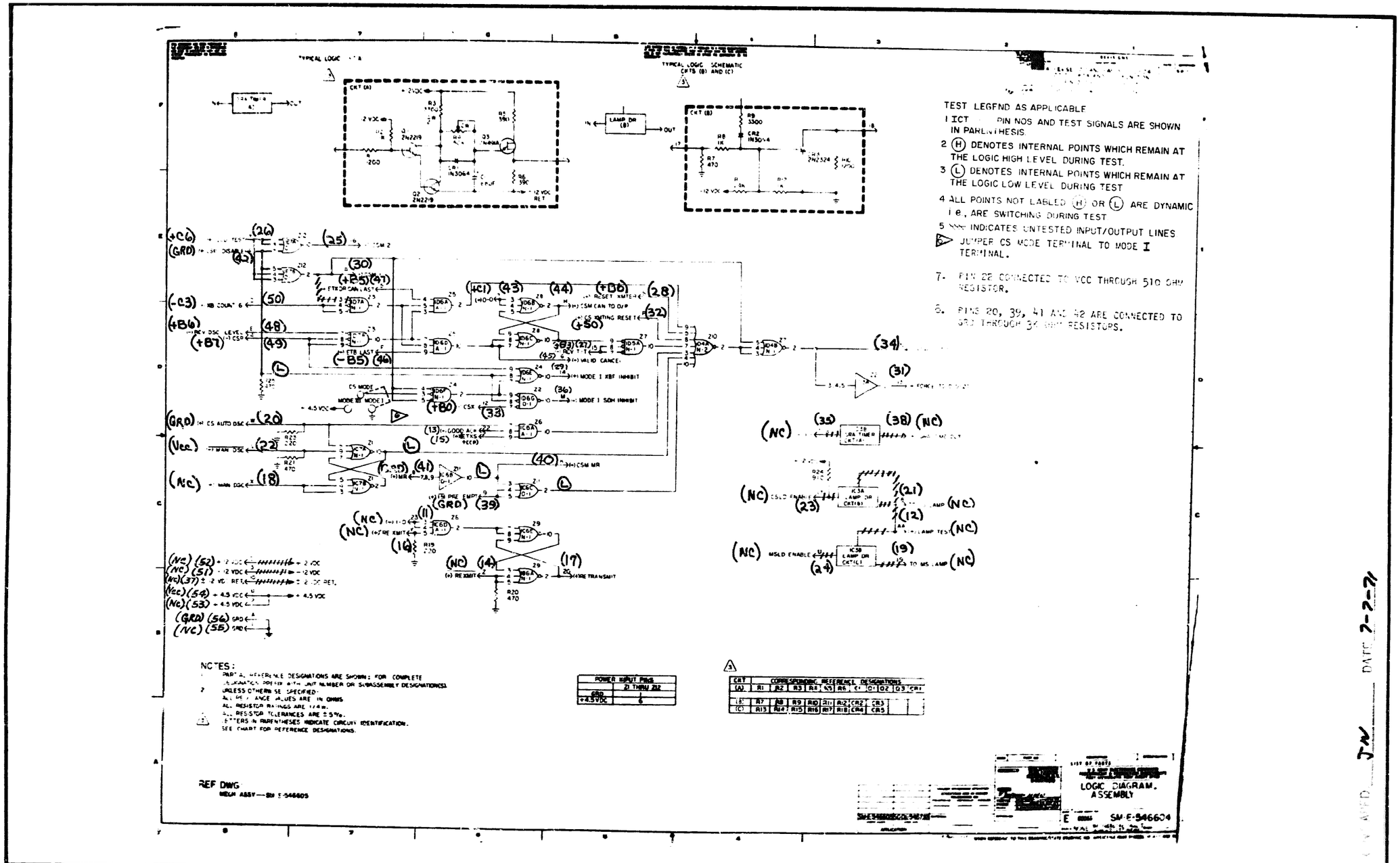
OUTPUT PINS (TEST POINTS)	SWITCH SETTING											
(17) ▷5	A	1	2	3	4							
	B	5	3	3	10							
(25) 30	A	1	2	3	4	5	6					
	B	2	2	6	NT	NT	5					
40	A	1	2									
	B	2	9									
(31) 34	A	1	2	3	4	5	6	7	8	9	10	11
	B	2	4	8	5	4	5	7	11	4	5	#
29, 36*	A	1	2	3	4	5	6					
	B	2	2	6	11	9	7					



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

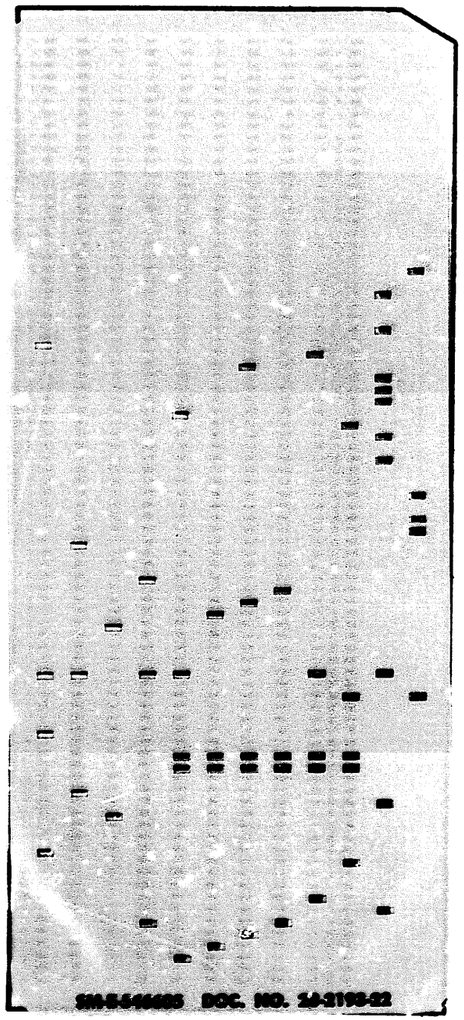
   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
5. ▷ BEFORE PROCEEDING WITH TEST PLACE A JUMPER FROM CS MODE TERMINAL TO MODE III TERMINAL.
6. NT INDICATES NO TEST.



P.C. Assembly SM-E-546605-001

P.C. Logic SM-E-546604

Doc. No. 23-2193-22



DYNATRONICS TESTAGRAM

TEST PARAMETERS

Vcc	+4.75	SIG	GRD. +VCC
+V		LOAD REF V	VCC GRD
+V		CLK	1 μ sec
-V		BIT CLK	+OSC

ROW ASSIGNMENT

	+B0
	-B3
2	+B5
3	+B6
4	+B7
5	+S0
6	-B5
7	-C3
8	+C1
9	+C0

INPUT PINS	COL	SIG
	63	+C0
43	64	-C1
	65	-C2
50	66	-C3
	67	-C4
	68	+C5
26	69	-C6
33	70	+B0
	71	+B1
	72	+B2
27	73	+B3
	74	+B4
46 , 47	75	+B5
48, 28	76	+B6
29	77	+B7
32	78	+S0
	79	+S1
	80	+S2
		+C0 REF

WAVEFORMS — ⟵ ⟶ 4 μ sec

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
29 ▷	A 1 2 / B 7 7
36	A 1 2 3 # / B 3 4 6 7
44	A 1 2 3 / B 5 5 #
45	A 1 2 3 / B 5 9 #
(31) 34	A 1 2 3 4 5 6 7 8 9 10 11 12 / B 2 8 10 1 3 3 7 9 5 NT NT 1

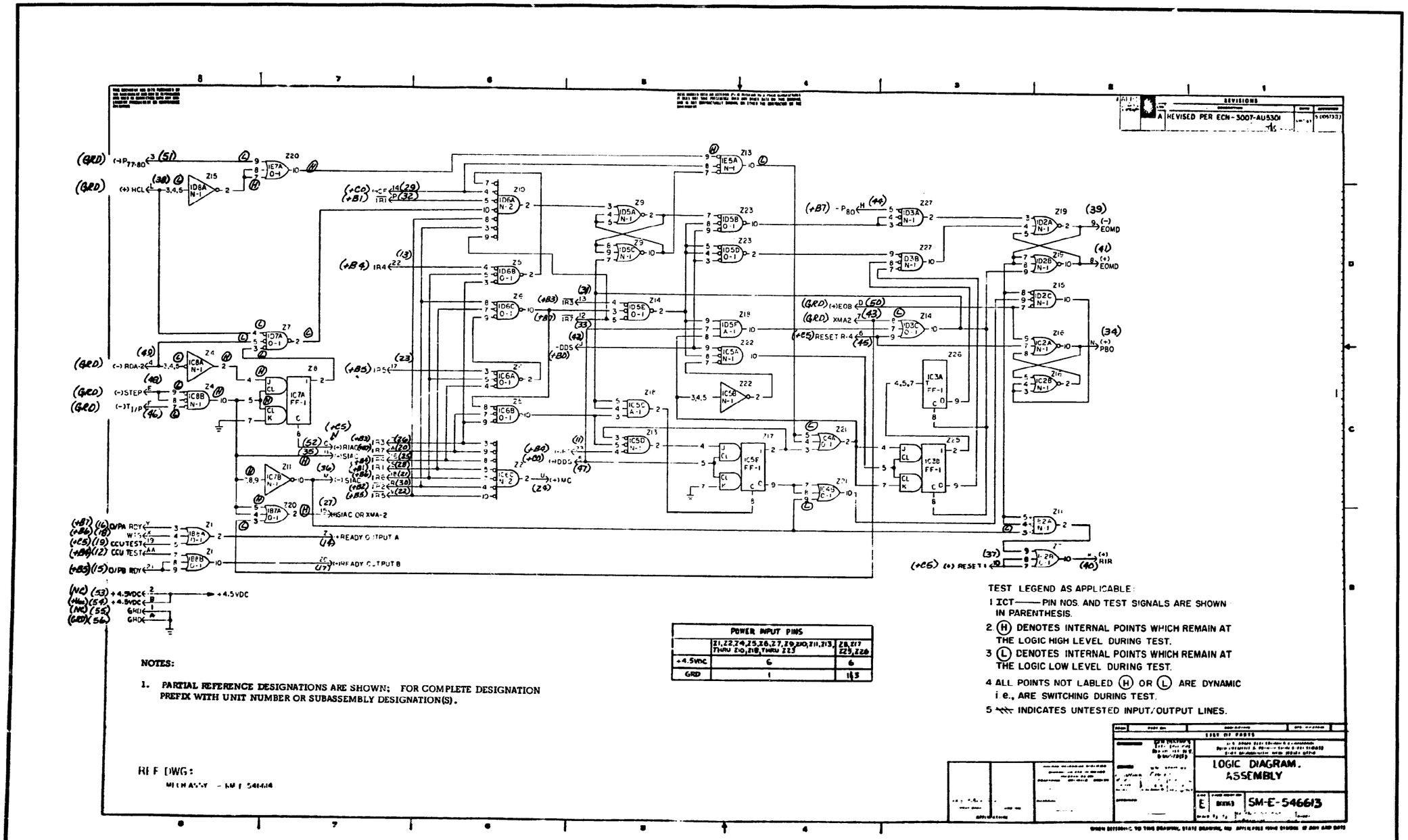
COPYRIGHT 1971 GENERAL DYNAMICS CORP. PRINTED IN U.S.A.

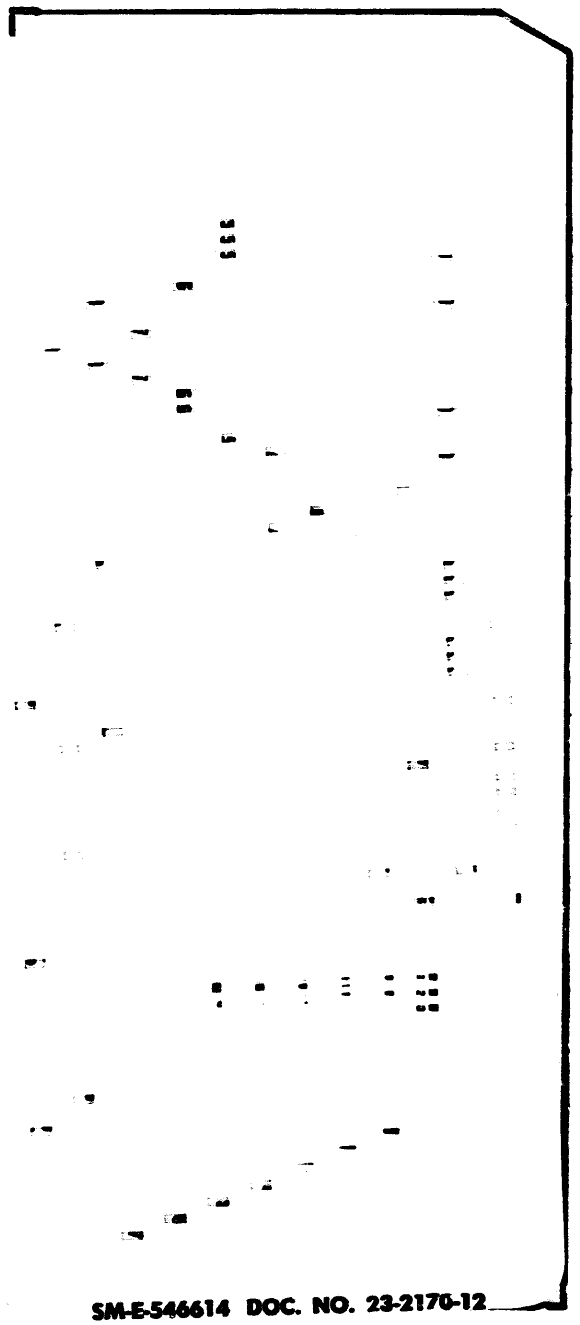
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
5. ▷ BEFORE PROCEEDING WITH TEST PLACE A JUMPER FROM CS MODE TERMINAL TO MODE 1 TERMINAL.
6. NT INDICATES NO TEST.

ENGR APPD. JN DATE 7-7-71


REVISIONS
A REVISED PER ECN-3007-AU5301
(+P77-80)
(+) HCL
(-) RDA-2
(-)STEP
(-)T1/P
(+)RIAC
(-)SIAC
XMSIAC OR XMA-2
(+)READY OUTPUT A
(+)READY OUTPUT B
O/PA RDY
O/PB RDY
CCU TEST
+4.5VDC
GND
(+)IR4
(+)IR5
(+)IR3
(+)IR7
(+)DDS
(+)MC
(+)IR1
(+)IR2
(+)IR6
(+)P80
XMA2
(+)EOB
RESET R-4
(-) EOMD
(+) EOMD
(+)PBO
(+)RIR
IC7A FF-1
IC8A N-1
IC8B N-1
IC7B N-1
IB7A O-1
IB8A N-1
IB8B O-1
ID8A N-1
ID7A O-1
ID6A N-2
ID6B O-1
ID6C O-1
ID5A N-1
ID5B O-1
ID5C N-1
ID5D O-1
ID5E O-1
ID5F A-1
IC5A N-1
IC5B N-1
IC5C A-1
IC5D N-1
IC5F FF-1
IC4A O-1
IC4B O-1
IE7A O-1
IE5A N-1
ID3A N-1
ID3B N-1
ID3C O-1
IC3A FF-1
IC3B FF-1
ID2A N-1
ID2B N-1
ID2C N-1
IC2A N-1
IC2B N-1
IC2C N-1
IE2A N-1
IE2B N-1
TEST LEGEND AS APPLICABLE:
1 ICT—PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5 INDICATES UNTESTED INPUT/OUTPUT LINES.
POWER INPUT PINS
+4.5VDC
GRD
LOGIC DIAGRAM. ASSEMBLY
SM-E-546613
NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
REF DWG:



TEST PARAMETERS			
V_{cc}	+4.75V	SIG V	+VCC, GRD
±V	—	LOAD REF V	1.2 GRD 1.1 VCC
+V	—	CLK	1 μ sec
-V	—	BIT CLK	+OSC

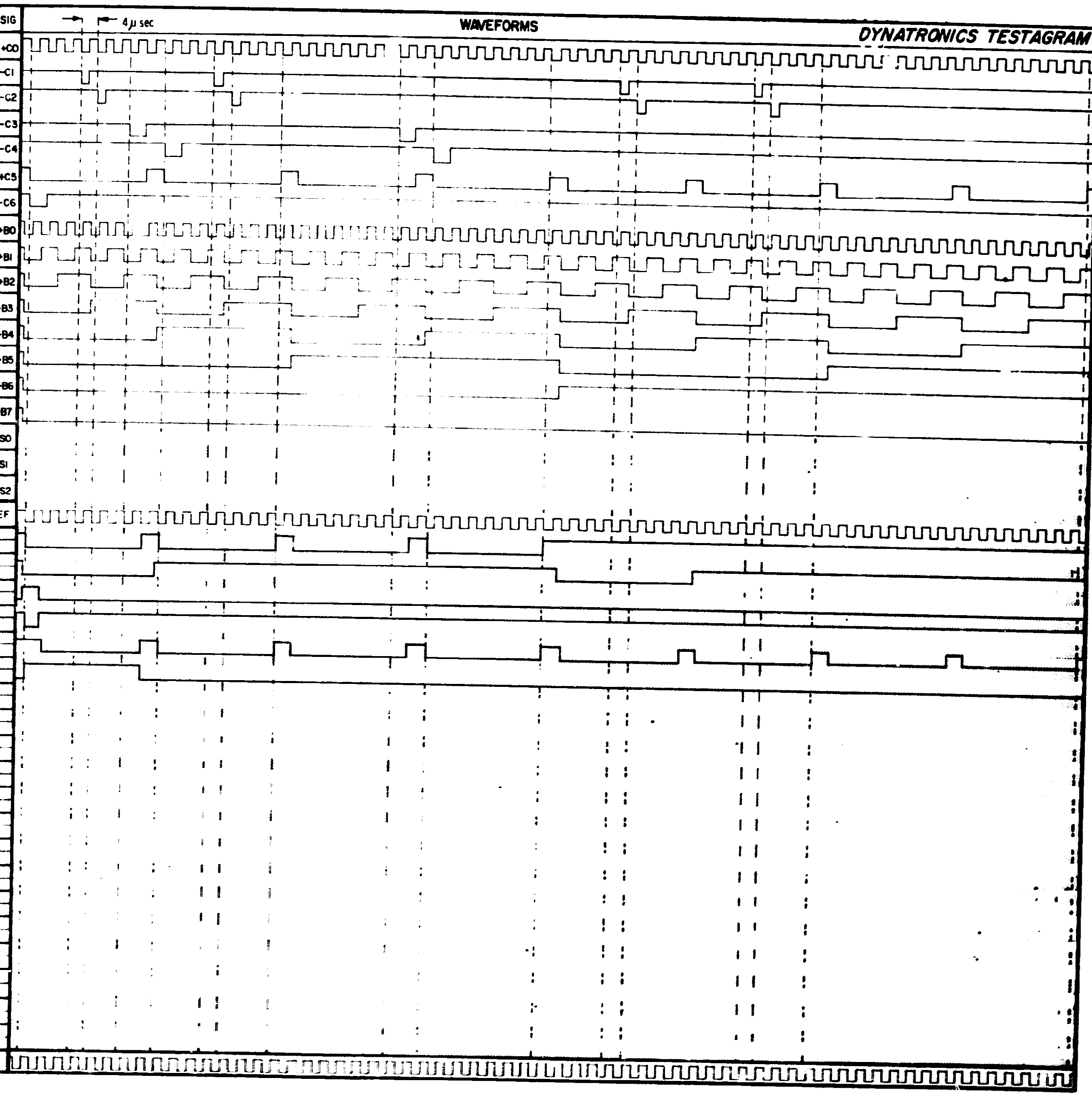
ROW ASSIGNMENT	
10	+C0
1	+B1
2	+B2
3	+B3
4	+B4
5	+B5
6	+B6
7	+B7
8	+C5
9	+B0

INPUT PINS	COL	SIG
29, 47	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
19, 37, 45, 52	68	+C5
	69	-C6
42	70	+B0
32, 28	71	+B1
30	72	+B2
26, 31	73	+B3
13, 25, 12, 11	74	+B4
23, 22, 15	75	+B5
21, 18	76	+B6
20, 33, 16, 44	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING									
14	A	1	2	3	4	5	6	7	8	9
	B	3	9	2	8	1	7	11	6	#
17	A	1	2	3	4					
	B	2	1	9	8					
(24)	A	1	2	3						
	B	2	6	#						
(39) 41*	A	1	2	3						
	B	3	6	#						
40	A	1	2	3	4					
	B	6	9	2	8					
(34)	A	1	2	3						
	B	3	9	#						

+C0 REF

+B0 REF



NOTES:

1. * DENOTES INVERTED SIGNAL.

2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

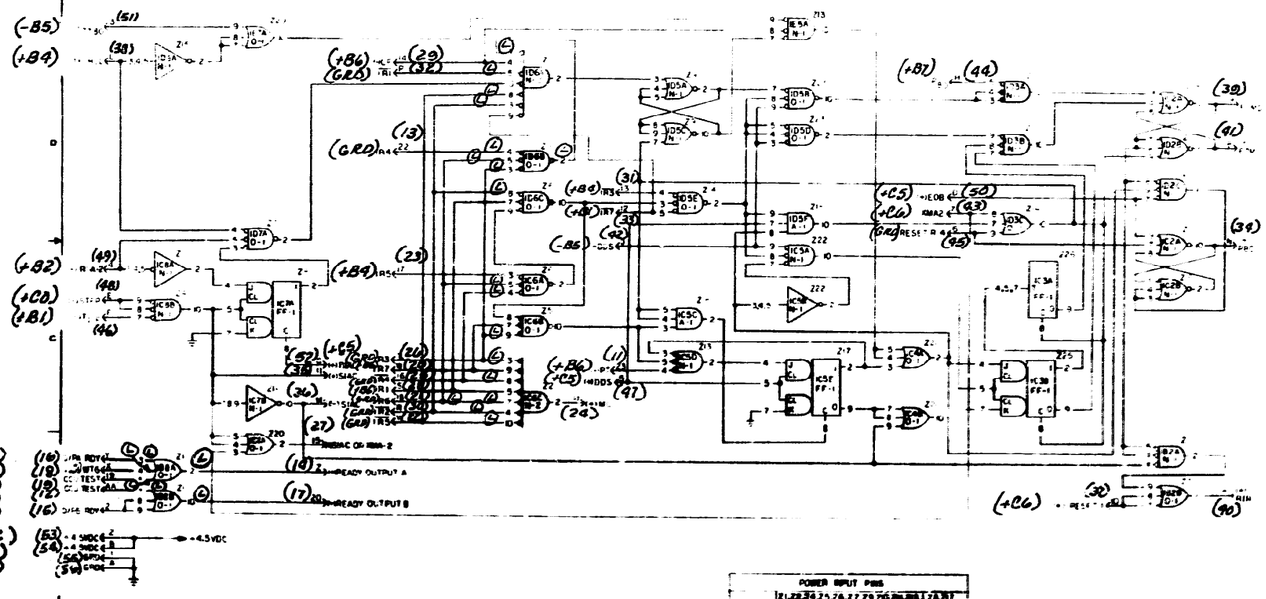
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.

4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

TEST LEGEND AS APPLICABLE.

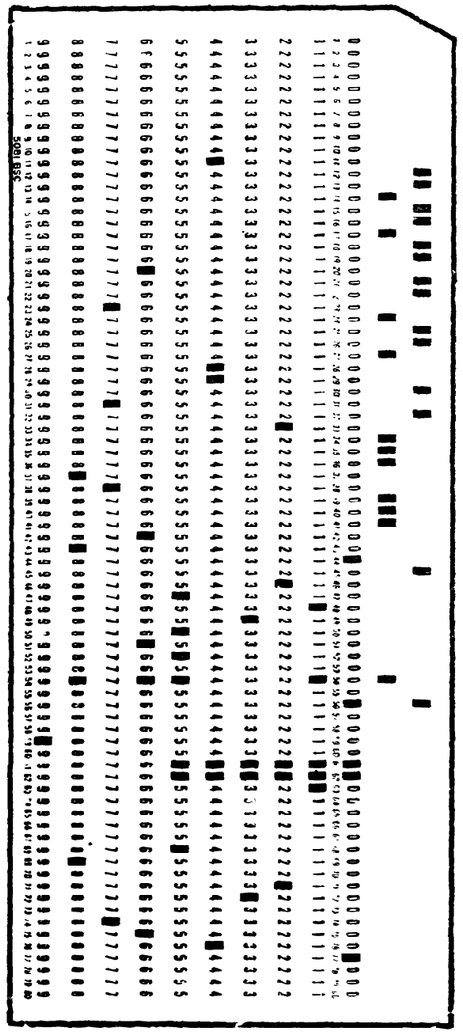
1. ICT—— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES



P.C. Assembly SM-E-546614

P.C. Logic SM-E-546613

Doc. No. 23-2170-22



TEST PARAMETERS			
V_{CC}	+4.75V	SIG V	+VCC GEN
+V	—	LOAD REF V	+2.5 GEN +VCC
+V	—	CLK	1 μ SEC
-V	—	BIT CLK	+05C

ROW ASSIGNMENT	
10	+B7
1	+C0
2	+B1
3	+B2
4	+B6
5	+C5
6	-B5
7	+B4
8	+C6
9	—

INPUT PINS	COL	SIG
48	63	+C0
	64	-C1
	65	-C2
		-C3
	67	-C4
47 50, 52	68	+C5
43*, 37*	69	-C6
	70	+B0
46 33	71	+B1
49	72	+B2
	73	+C3
23, 38, 31	74	+B4
20* 42*, 51*	75	+B5
29 28 11	76	+B6
44	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS) — SWITCH SETTING — +C0 REF

(39) 81*
34
35 36*
27
(41)

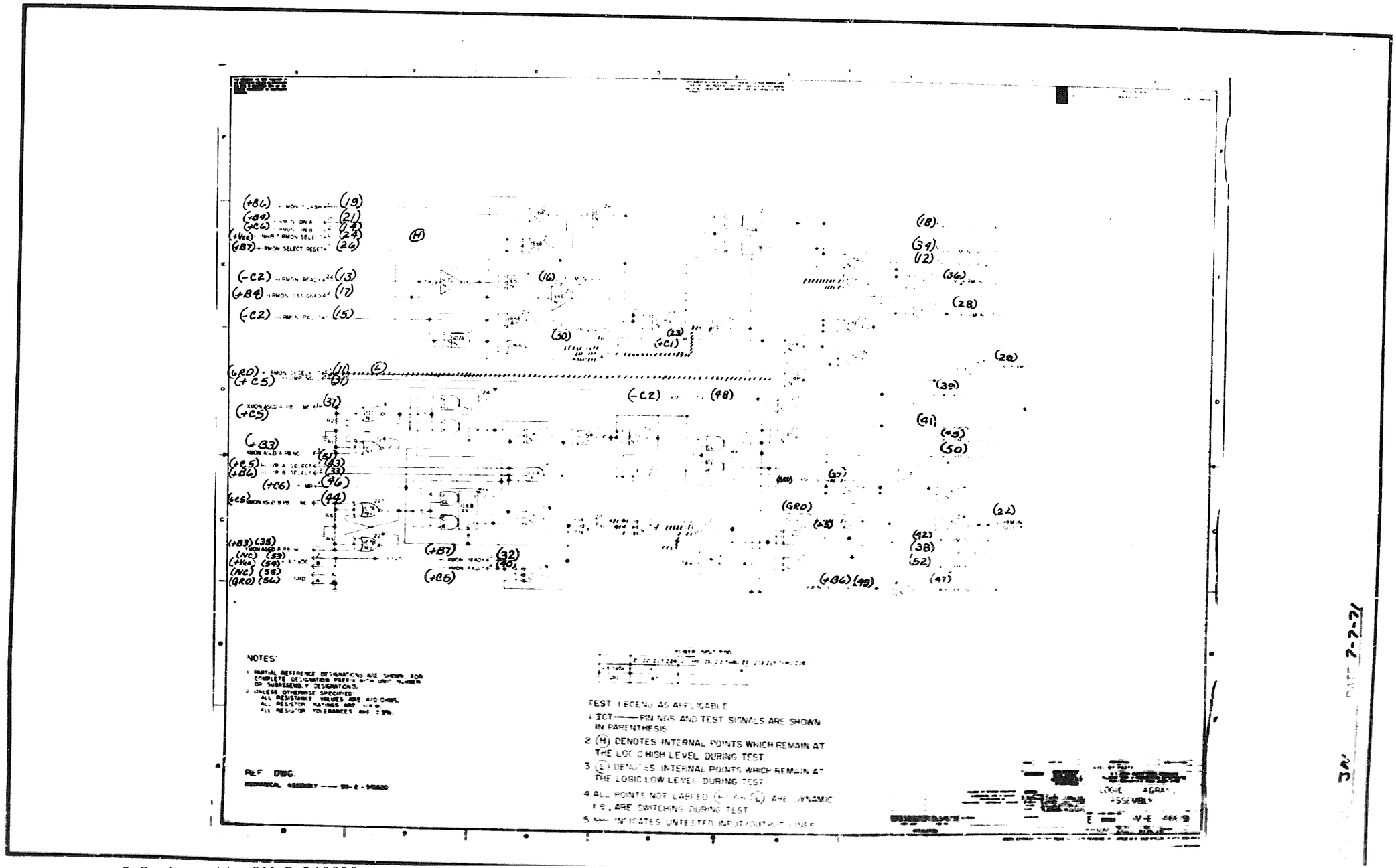
WAVEFORMS — 4 μ SEC — DYNATRONICS TESTAGRAM

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

GOVT APPD. JN DATE 7-2-71



P.C. Assembly SM-E-546620

P.C. Logic SM-E-546619

TEST PARAMETERS

Vcc	+.75V	SIG V	+VCC GRD
±V	—	LOAD REF V	12, GRD 11, VCC
+V	—	CLK	1 μ SEC
-V	—	BIT CLK	÷OSC

ROW ASSIGNMENT

10	+C5
—	-C2
2	+B4
3	+B6
4	+B7
5	+B3
6	+C0
7	+C1
8	—
9	—

INPUT PINS	COL	SIG
	63	+C0
23*	64	-C1
13, 15, 48	65	-C2
	66	-C3
	67	C4
11, 37, 43, 44, 40	68	+C5
14*, 46*	69	-C6
	70	+B0
	71	+B1
	72	+B2
51, 35	73	+B3
21, 17	74	+B4
	75	+B5
19, 33, 49	76	+B6
26, 32	77	+B7
	78	+S0
	79	+S1
	80	+S2

WAVEFORMS — ← → 4 μ sec — DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS)	SWITCH SETTING	+CO REF
16		
30		
24		
(18) 34		
28		
12		
(36)		
47		
29		
39, 41		
45		
50		
22		
42		
38		
52		

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.
   IN ICT-103 TESTER PRESS "B" SWITCH WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

SM-E-546620 DOC. NO. 23-2171-11

GOVT APPD. JN DATE 7-7-71

TEST LEGEND AS APPLICABLE:

1. ICT ____ PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ≈≈ INDICATES UNTESTED INPUT/OUTPUT LINES

NOTES:

1. PARTIAL REFERENCE DESIGNATORS ARE SHOWN FOR CONCISE DESIGNATION. PREFIX EXISTS ONLY WHERE NUMBER OF SUBSYSTEMS DESIGNATED.

REF DWG:

MECH ASSY — SM-E-546623

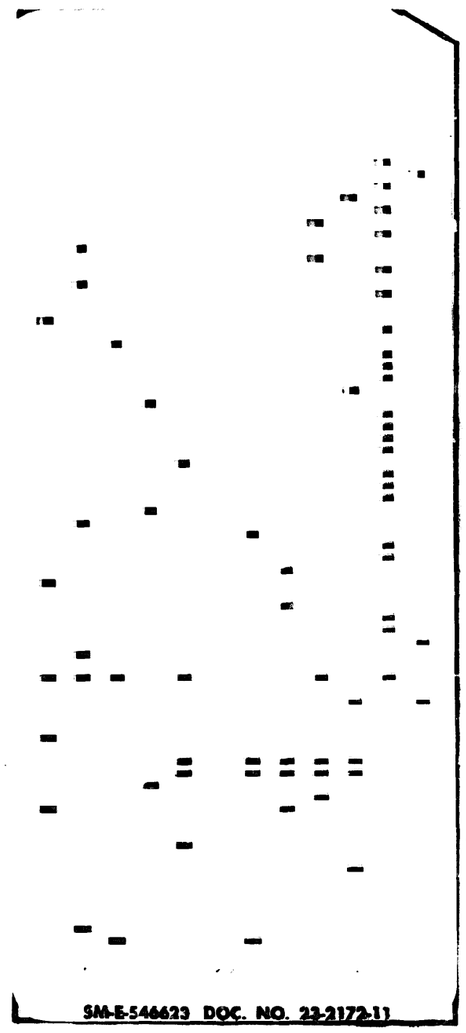
POWER INPUT PINS	
	PIN NO.
+4.5VDC	5
GND	1

LOGIC DIAGRAM, ASSEMBLY

SM-E-546622

JM 2-2-71

P.C. Assembly SM-E-546623
P.C. Logic SM-E-546622



SM-E-546623 DOC. NO. 23-2172-11

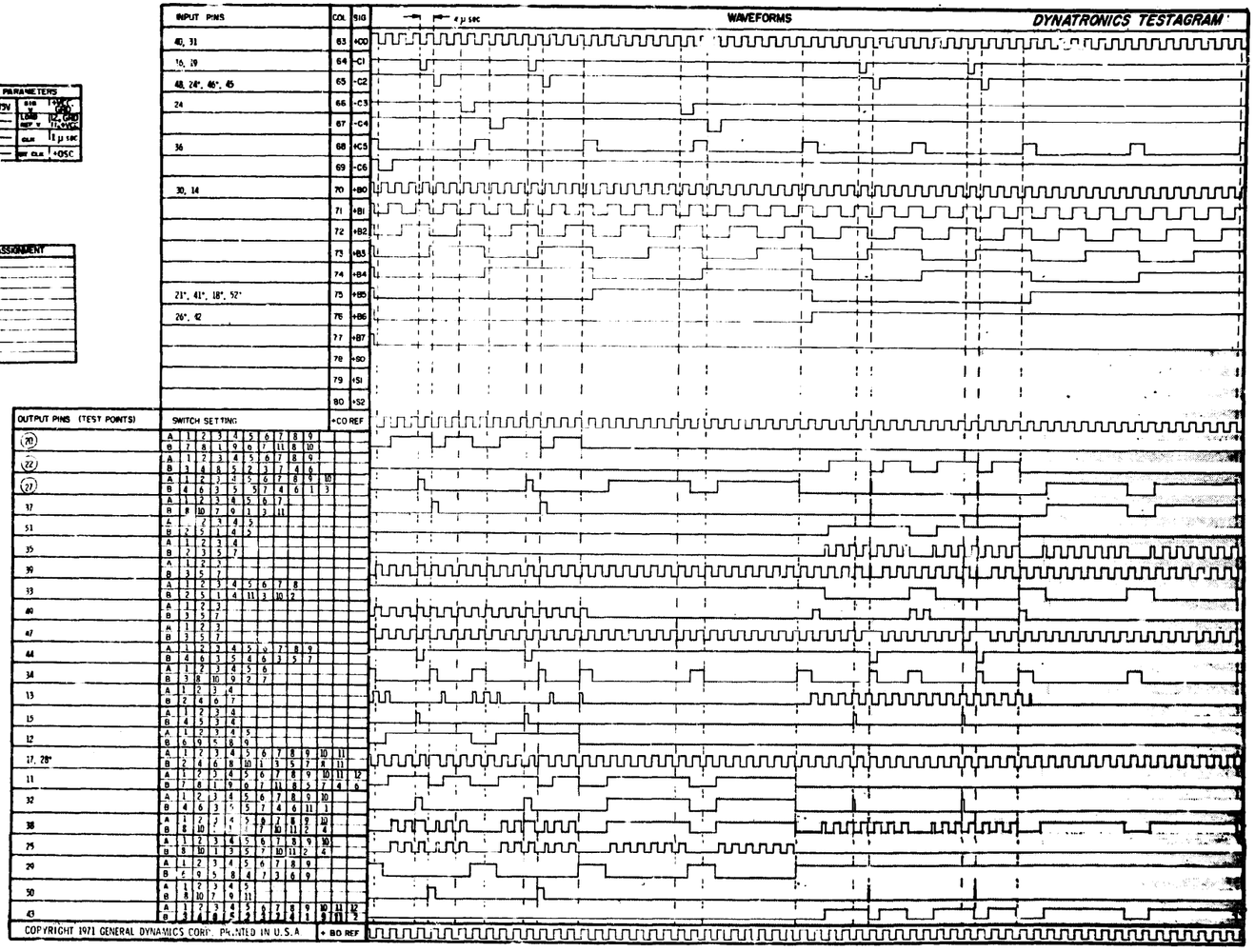
GOVT APPD. JN DATE 7-7-71

TEST PARAMETERS

V_{cc}	+4.75V	CLK	250K 50%
+V	—	LOAD	DC GND
+V	—	REF V	TTL LEVEL
+V	—	CLK	1 μ sec
-V	—	REF CLK	+05C

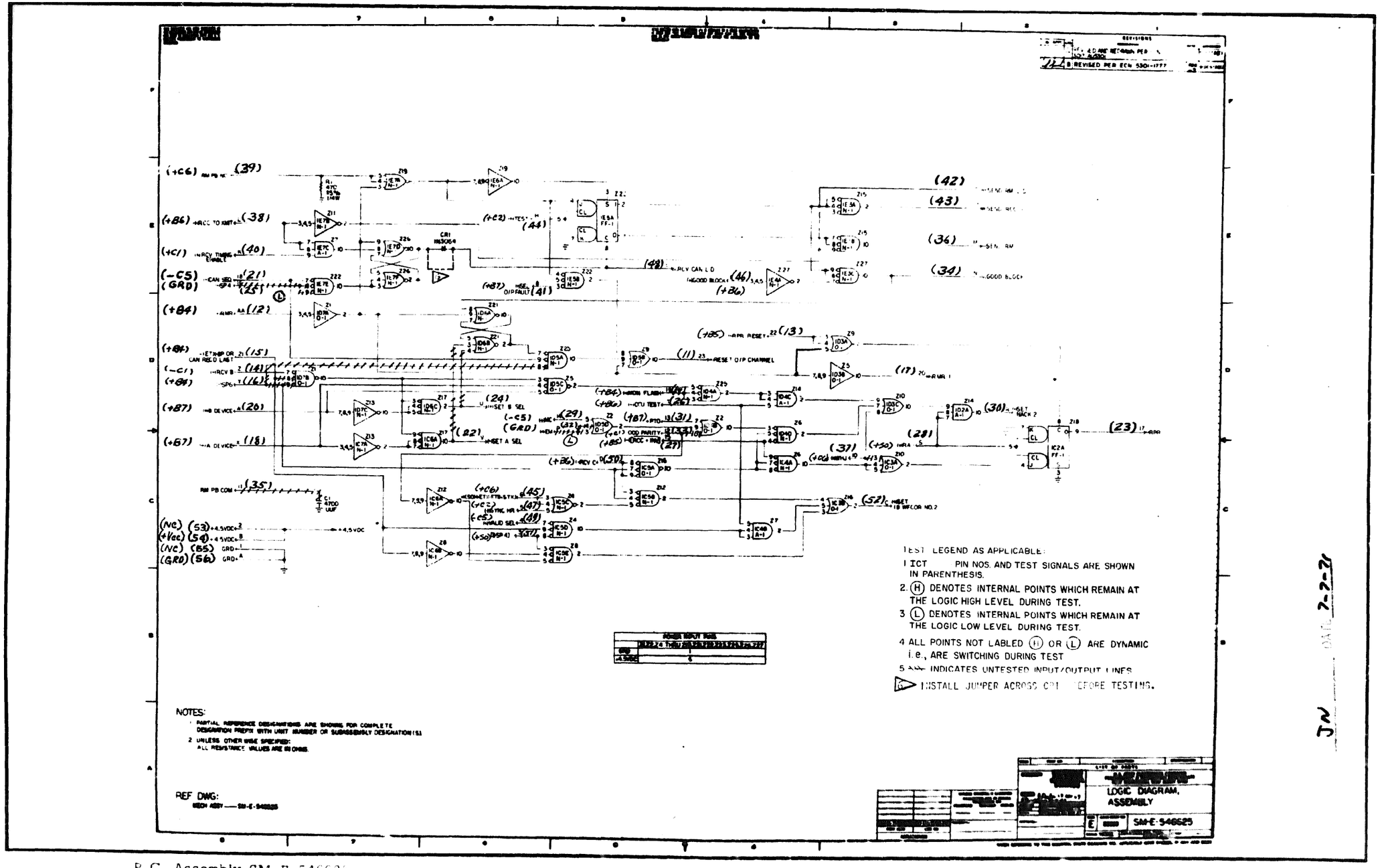
ROW ASSIGNMENT

10	+B0
1	-C1
2	-C7
3	+B6
4	—
5	+C5
6	+C0
7	-B4
8	-B3
9	+C2



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.



P.C. Assembly SM-E-546626

P.C. Logic SM-E-546625

SM-E-546626 DOC. NO. 23-2173-11

GOVT APPD. JN DATE 2-2-71

TEST PARAMETERS

+Vcc	+4.75 V	SIG V	PWEC 250
+V	—	LOAD REF V	2V/250
+V	—	CLK	1 μ sec
-V	—	BIT CLK	+OSC

ROW ASSIGNMENT

10	C1
1	+S0
2	+B4
3	+B5
4	+B6
5	+B7
6	+C2
7	+C1
8	+C5
9	+C6

INPUT PINS	COL	SIG
	63	+C0
14, 33*, 43*	64	+C1
44, 5	65	+C2
	66	+C3
	67	+C4
21*, 60, 29	68	+C5
30*, 37, 45	69	+C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
17, 16, 9, 15	74	+B4
12, 27	75	+B5
46, 36, 20, 38	76	+B6
26, 18, 31, 41	77	+B7
28, 51	78	+S0
	79	+S1
	80	+S2

WAVEFORMS — 4 μ sec

DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
48 (5)	
22, 24	
42	
34, (43)	
36	
(11)	
17	
(30)	
(23)	
(52)	

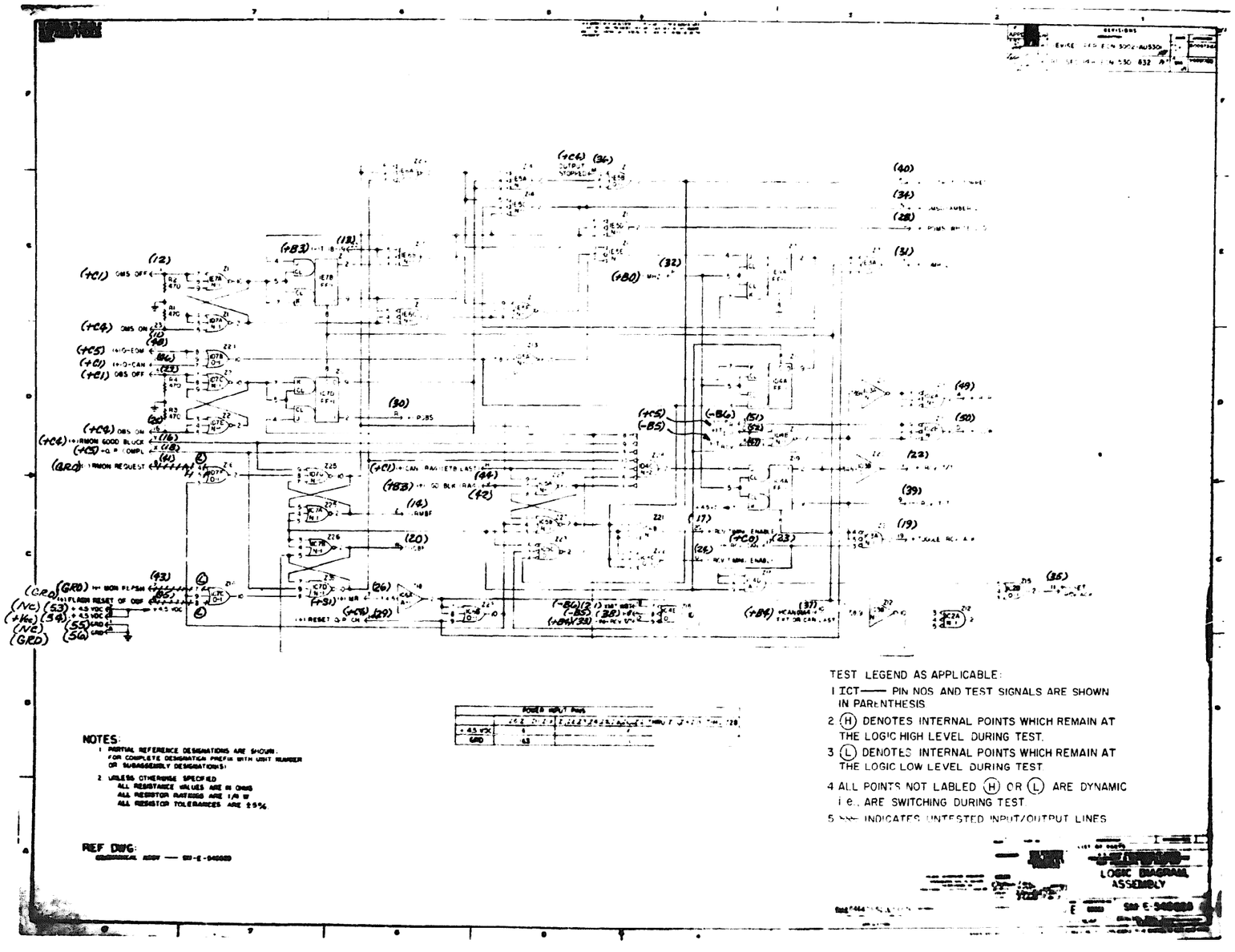
+C0 REF

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#": VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

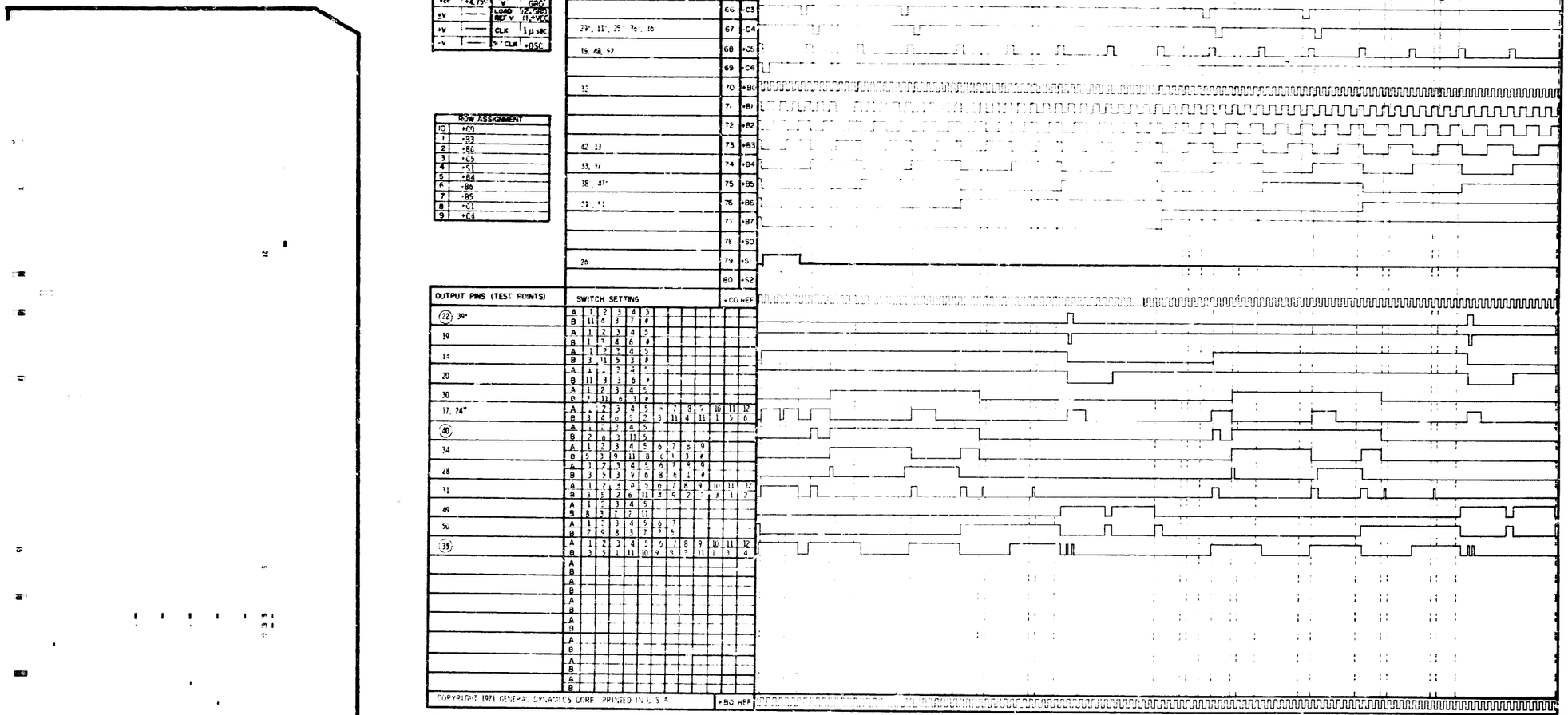
(5) INSTALL JUMPER ACROSS CR1 BEFORE TESTING.



P.C. Assembly SM-E-546629
P.C. Logic SM-E-546628

Doc. No. 2171-11

5 50 0



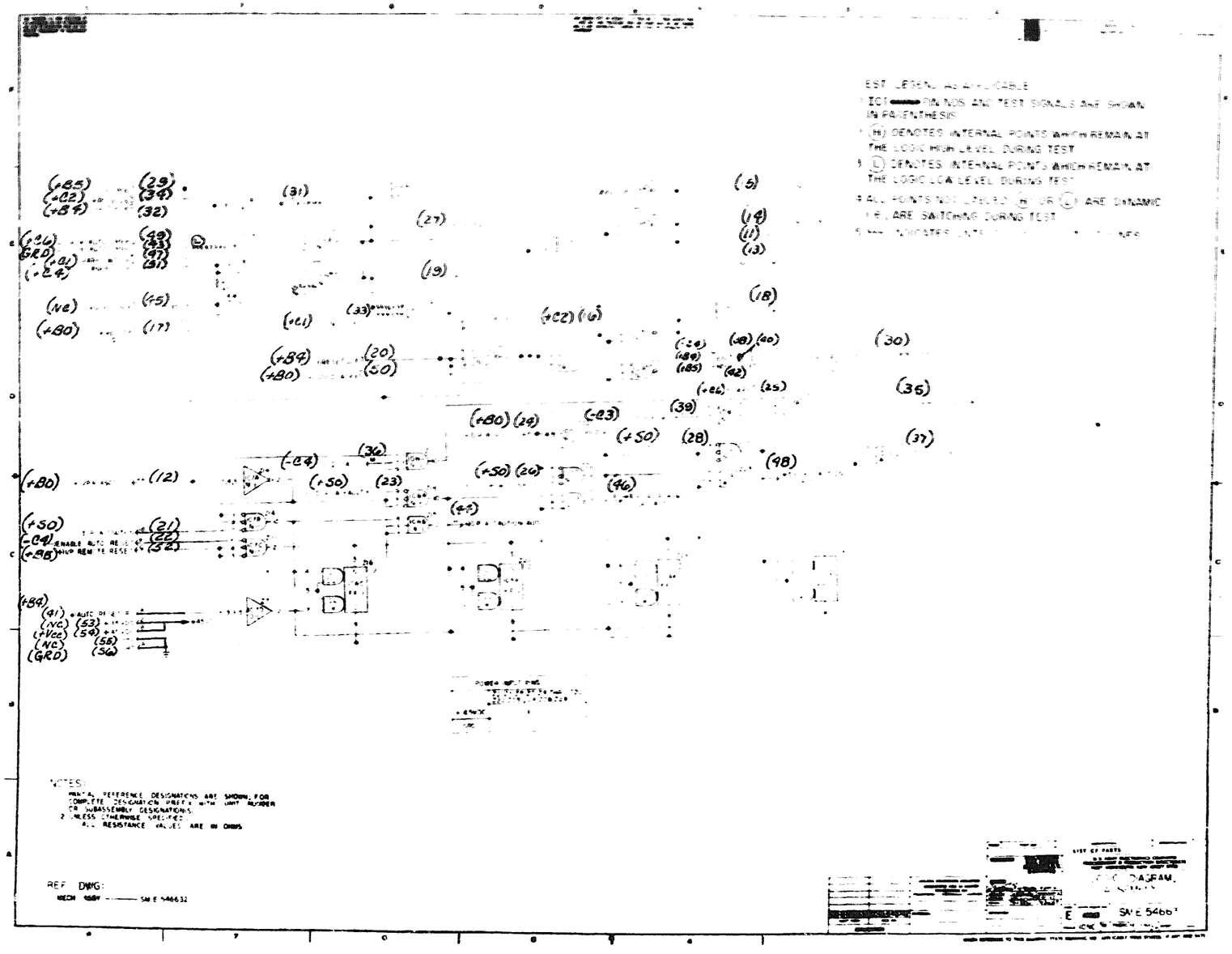
SM-E-546629 DOC. NO. 23-2174-11

GOVT APPD. JN DATE 7-7-71

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.



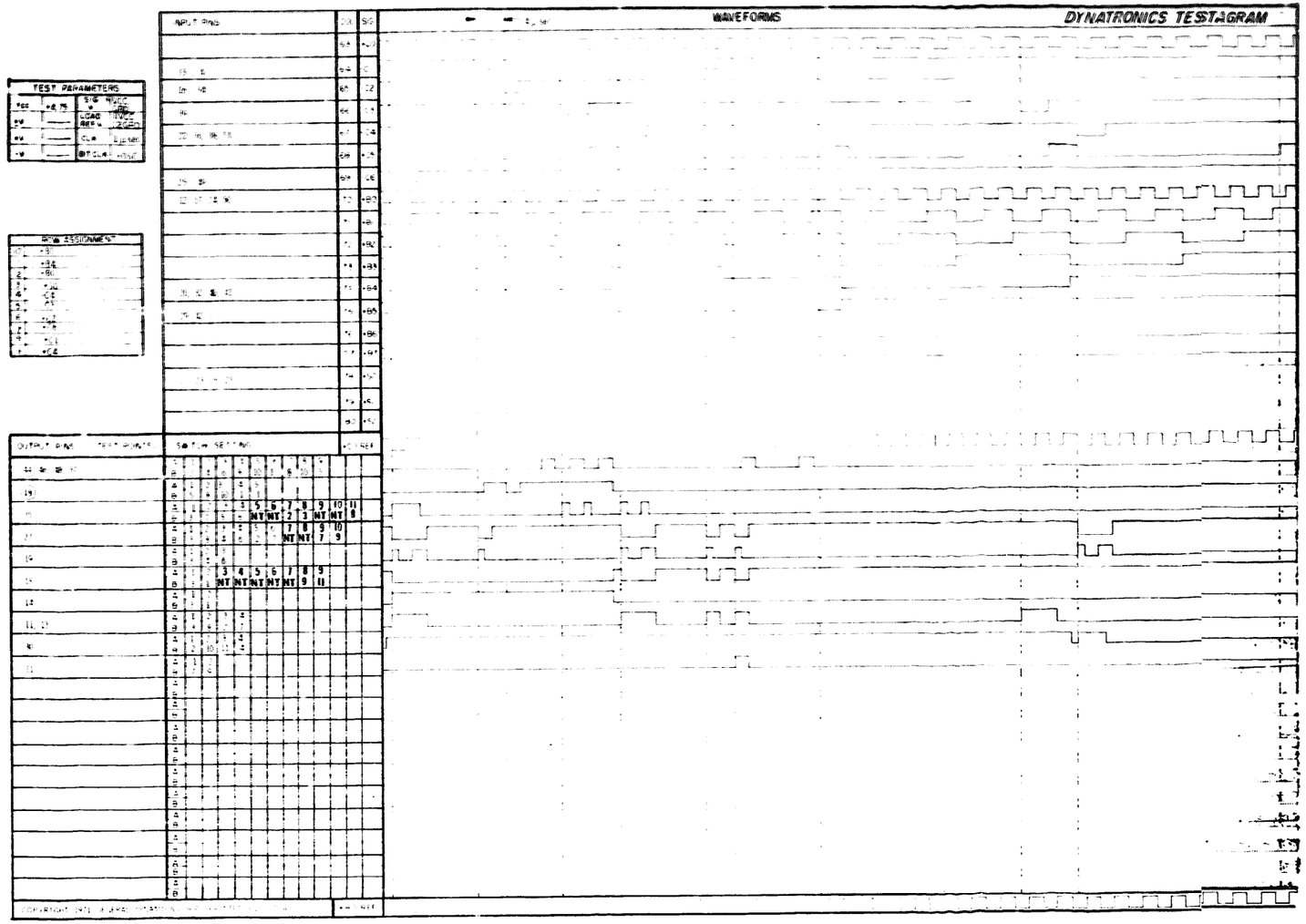
2-2-71

JN

P.C. Assembly SM-E-546632

5 2 P.C. Logic SM-E-546631 Doc. No. 23-2173-11

SM-E-546632 DOC. NO. 23-2175-11



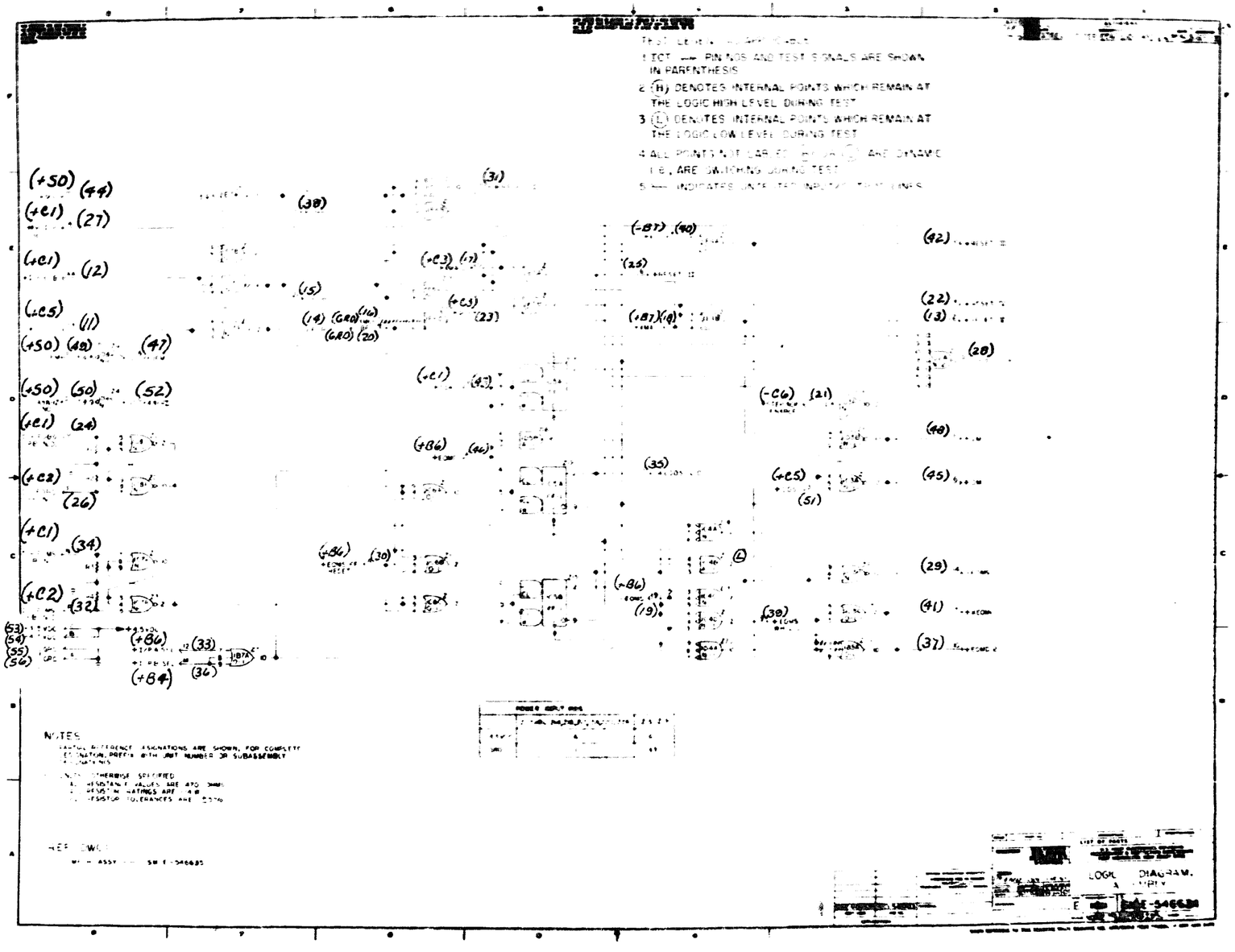
NOTES:

1. *DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. NT INDICATES NO TEST.

DRAWN JN 7-7-71

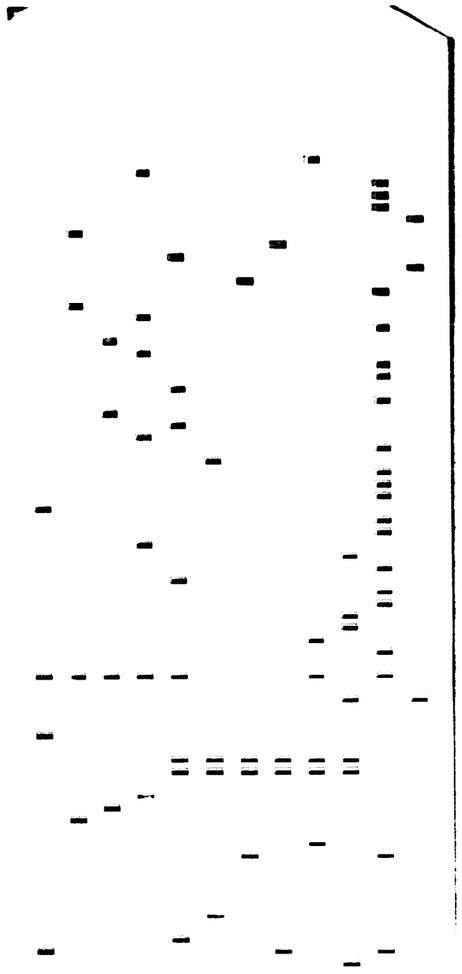
Doc. No. 23- 2175-11

P.C. Assembly SM-E-546632
P.C. Logic SM-E-546631



P.C. Assembly SM-E-546635

5 4 P.C. Logic SM-E-546634 Doc. No. 2170-12



SM-E-546635 DOC. NO. 23-2176-12

GOVT APPD. JN DATE 7-7-71

TEST PARAMETERS

V_{CC}	+4.75%	SIG V	+2.4V / +0.4V
+V	—	LOAD REF V	IOZ = ±100 µA, VOZ = +2.4V
+V	—	CLK	1 µ sec
-V	—	REF CLK	+05C

ROW ASSIGNMENT

0	+S0
1	+C5
2	+B7
3	-C6
4	+B4
5	+B6
6	+C1
7	+C2
8	+C3
9	-B7

INPUT PINS	COL	SIG
	63	+C0
17, 24, 34, 77, 43	64	-C1
26, 32	65	-C2
12, 23	66	-C3
	67	-C4
11, 51	68	+C5
21	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
36	74	+B4
	75	+B5
46, 19, 33, 30	76	+B6
10, 18	77	+B7
44, 49, 50	78	+S0
	79	+S1
	80	+S2
SWITCH SETTING	+C0 REF	

OUTPUT PINS (TEST POINTS)

18, 31, 47*, 52*

22, 25

42

(15)

14

13

(28)

(48)

45

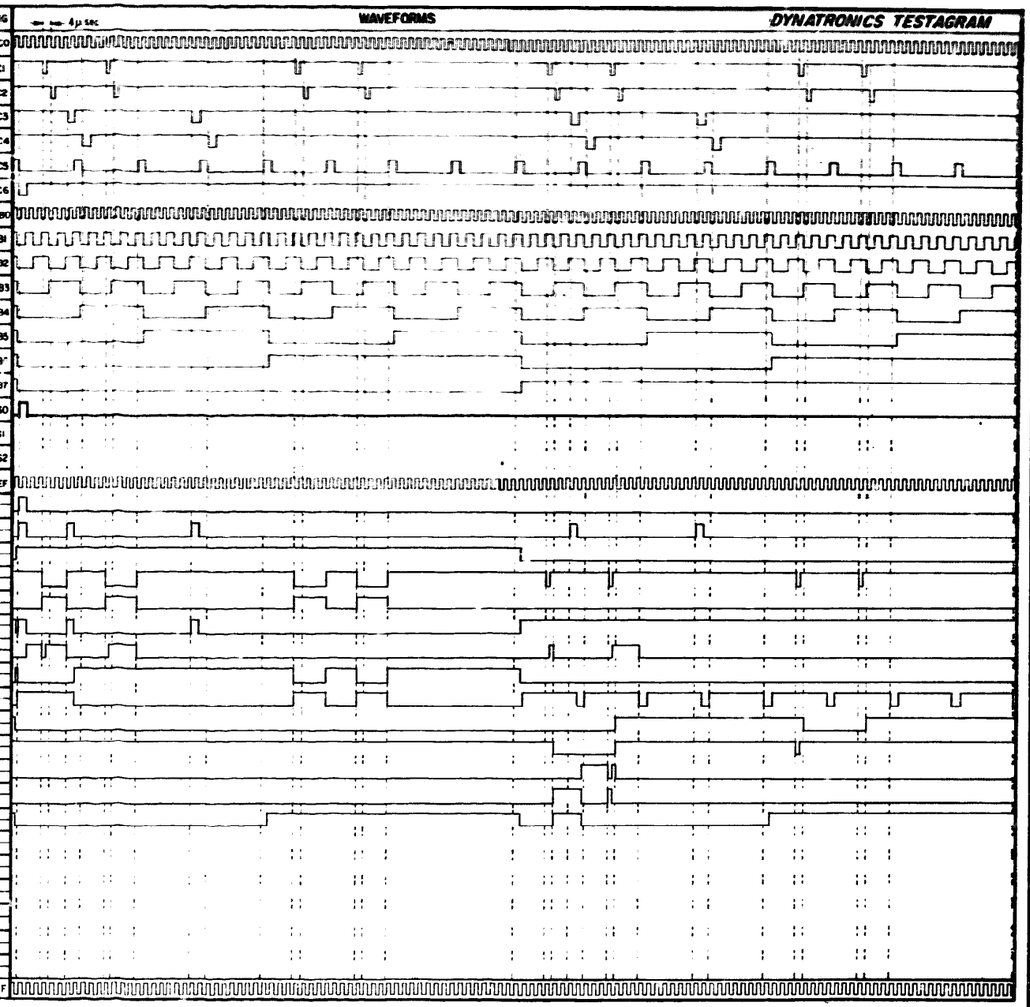
(35)

(29)

39

(41)

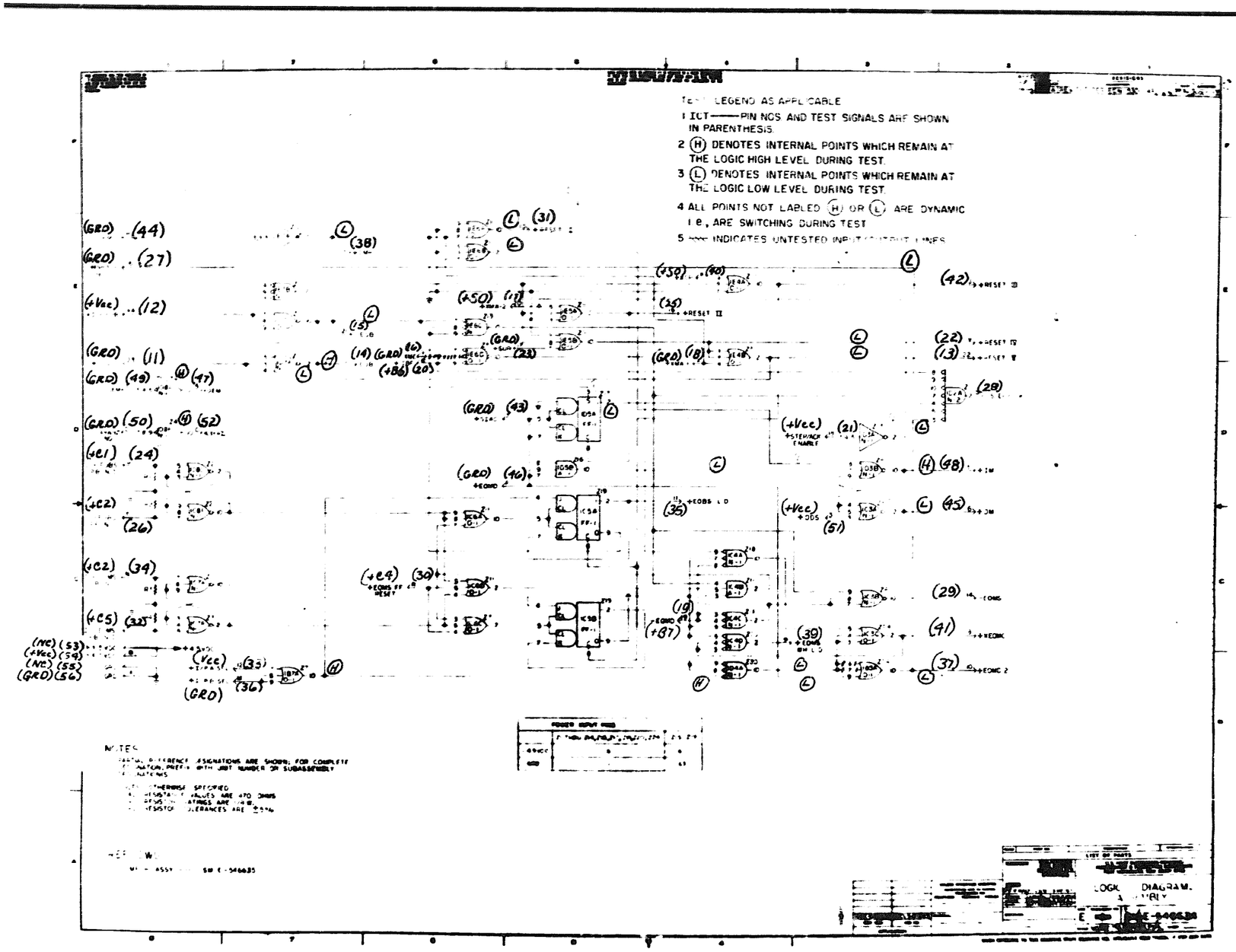
(37)



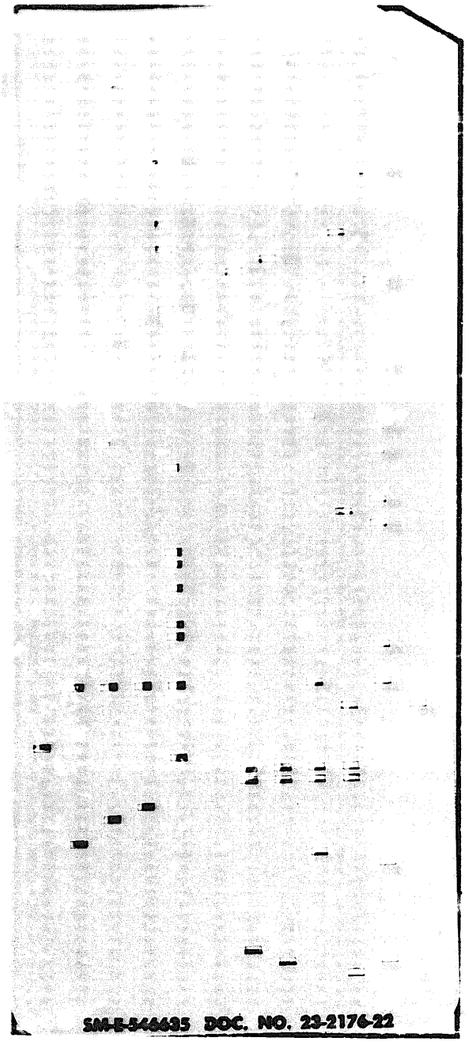
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.



P. C. Assembly SM-E-546635
P.C. Logic SM-E-546634



TEST PARAMETERS

Vcc	+4.75V	SIG	PULSE
+V		LOAD REP.	12 usec WIDTH
+V		CLR	1 μ sec
-V		SET CLR	HOSE

PIN ASSIGNMENT

10	+S0
2	+S1
3	+S2
4	
5	GND
6	+B1
7	+B2
8	+B3
9	+B4

INPUT PINS

	63	+CO
10	64	C1
12 10	65	C2
	66	C3
11	67	C4
10	68	+C5
	69	+C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
11	76	+B6
15	77	+B7
17 18	78	+S0
	79	+S1
	80	+S2

WAVEFORMS — DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS) — SWITCH SETTING — +CO REF

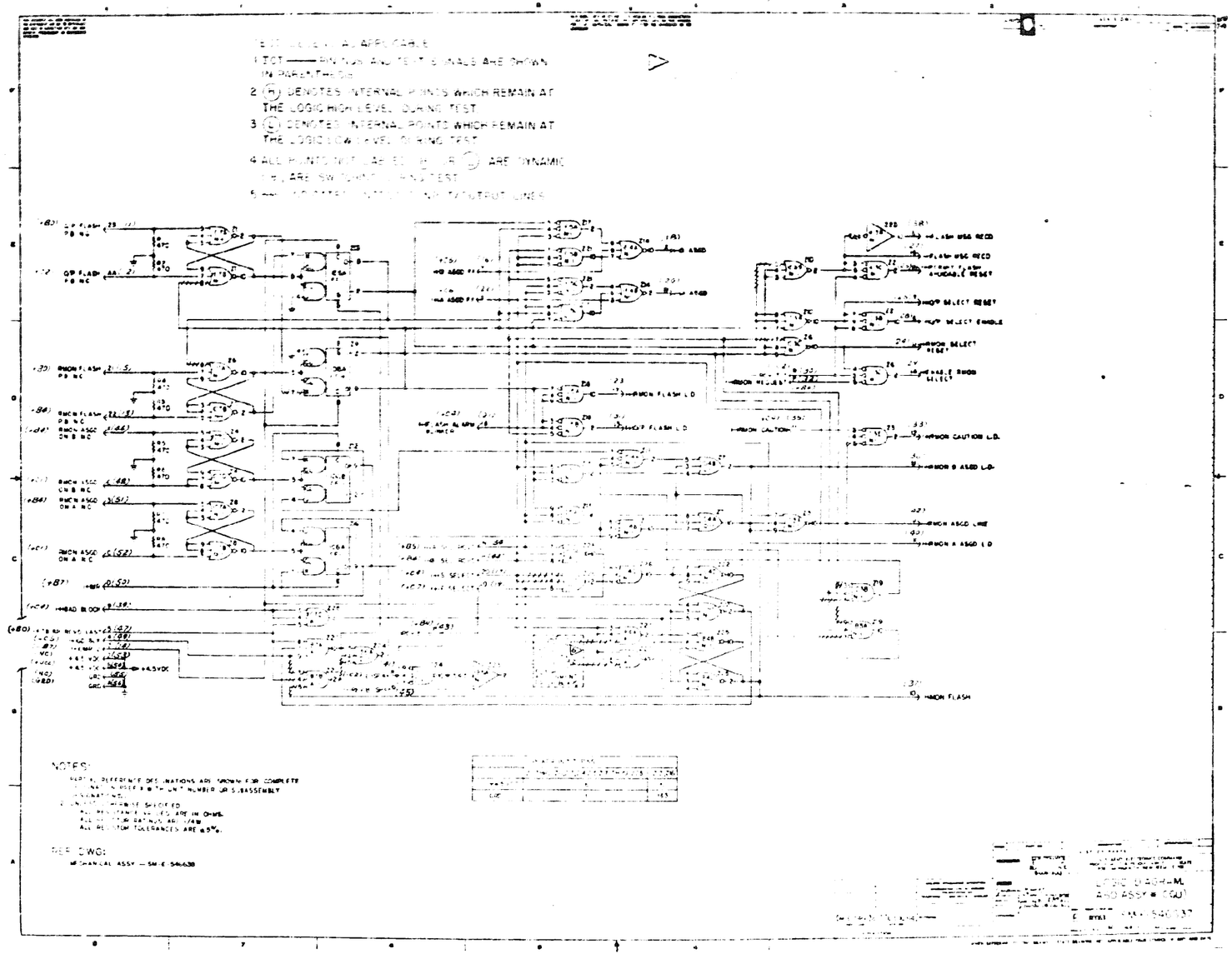
13	A	1	2	3	4	5	6	7	8	9	10	11	12
	B	2	4	6	8	10	12	14	16	18	20	22	24
15	A	1	2	3	4	5	6	7	8	9	10	11	#
	B	3	5	7	9	11	13	15	17	19	21	23	
41	A												
	B	0	4	6	8								
16	A	1	2	3	4	5	6	7	8	9			
	B	3	4	5	9	11	13	15	17	19			
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												
	A												
	B												

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO, NO-GO TESTED FIRST.

GOVT APPD. JN DATE 2-2-71



P.C. Assembly SM-E-5[illegible]

P.C. Logic SM-E-54[illegible]

SM-E-546638 DOC. NO. 23-2177-12

GOVT APPD. JN DATE 7-7-71

TEST PARAMETERS

V_{CC}	+4.75	SIG	t_1 VCC t_2
+V	—	LOAD REF V	t_1 VCC t_2
+V	—	CLR	1 μ sec
-V	—	KEY CLK	+ OSC

ROW ASSIGNMENT

IC	+C5
1	+B0
2	+B4
3	+B5
4	+B7
5	-C2
6	+C1
7	+C6
8	+C4
9	+C2

INPUT PINS	COL	SIG
	63	+C0
65, 52	64	-C1
30, 41, 12, 19	65	-C2
	66	-C3
17, 21, 35, 55	67	-C4
45	68	+C5
16, 22	69	+C6
11, 15, 47	70	+B0
	71	+B1
	72	+B2
	73	+B3
13, 32, 43, 44, 46	74	+B4
34	75	+B5
	76	+B6
14, 50	77	+B7
	78	+S0
	79	+S1
	80	+S2

WAVEFORMS — DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS)	SWITCH SETTING	+CO REF
⑫	A 1 2 3 4 / B 6 10 9 5	
37 ▷5	A 1 2 3 4 / B 8 3 4 5	
18	A 1 2 3 4 5 6 7 8 9 10 11 / B 3 NT 10 NT 11 NT NT NT 7 6 #	
20	A 1 2 3 4 5 6 / B 3 7 10 11 9 7	
36	A 1 2 3 4 5 6 7 / B 4 3 11 10 9 5 #	
27, 38*	A 1 2 3 / B 10 5 #	
25	A 1 2 / B 7 9	
28	A 1 2 3 / B 8 10 11	
26	A 1 2 / B 1 6	
29, 45	A 1 2 3 / B 8 NT 4	
33	A 1 2 / B 4 7	
31	A 1 2 3 / B 10 1 6	
23	A 1 2 3 4 5 6 / B 10 NT NT 4 5	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
5. ▷5 JUMPER ACROSS PINS 2 AND GRD ON FLASH ASSIGNMENT PATCH BOARD PRIOR TO TEST.
6. NT INDICATES NO TEST.

TEST LEGEND AS APPLICABLE

1 ICT——PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.

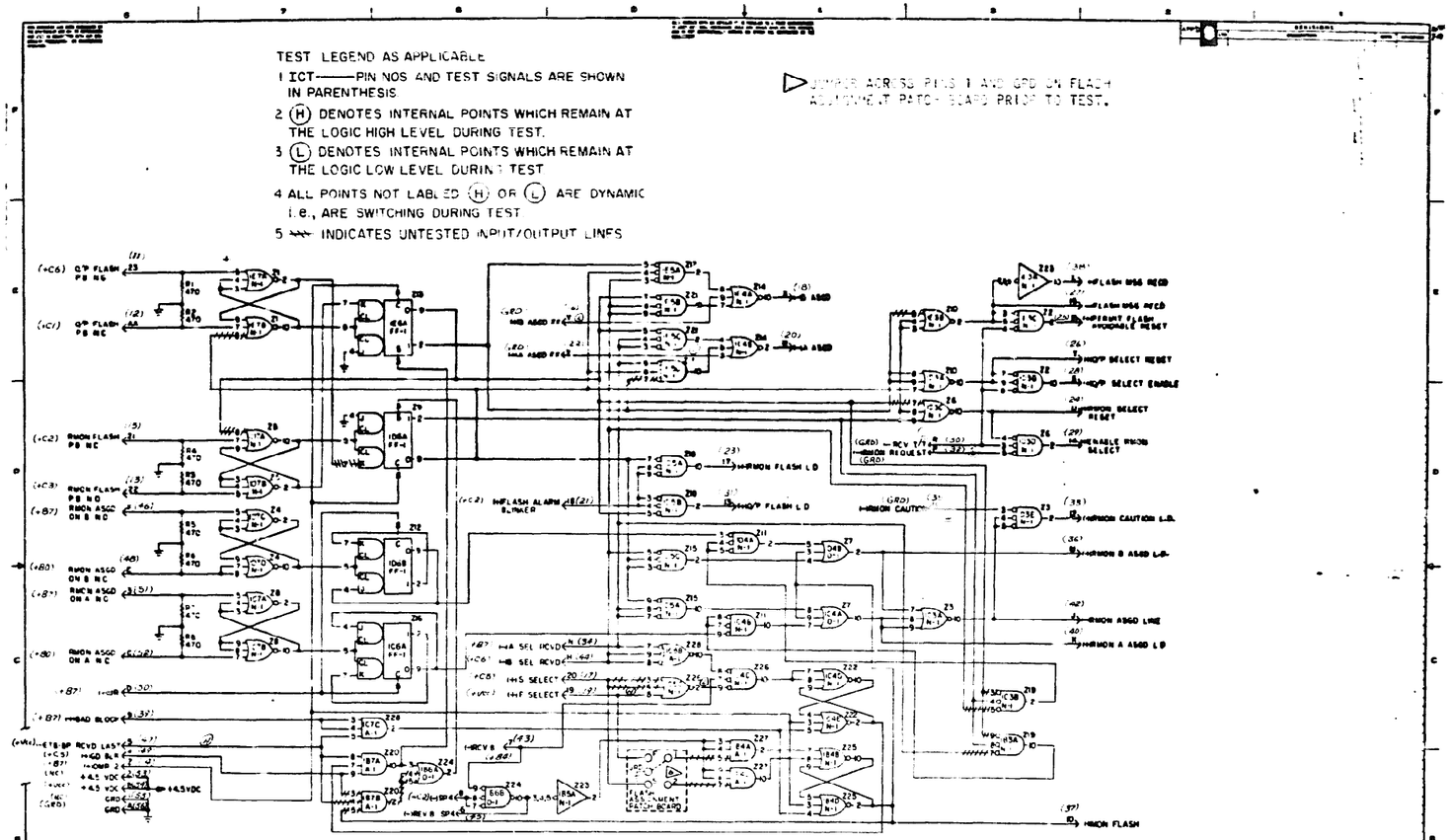
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES

▷ JUMPER ACROSS PINS 1 AND GRD ON FLASH ADJUSTMENT PATCH BOARD PRIOR TO TEST.



NOTES:

1. PART AL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR RATINGS ARE 1/4W.
   ALL RESISTOR TOLERANCES ARE ±5%.

REF DWG:

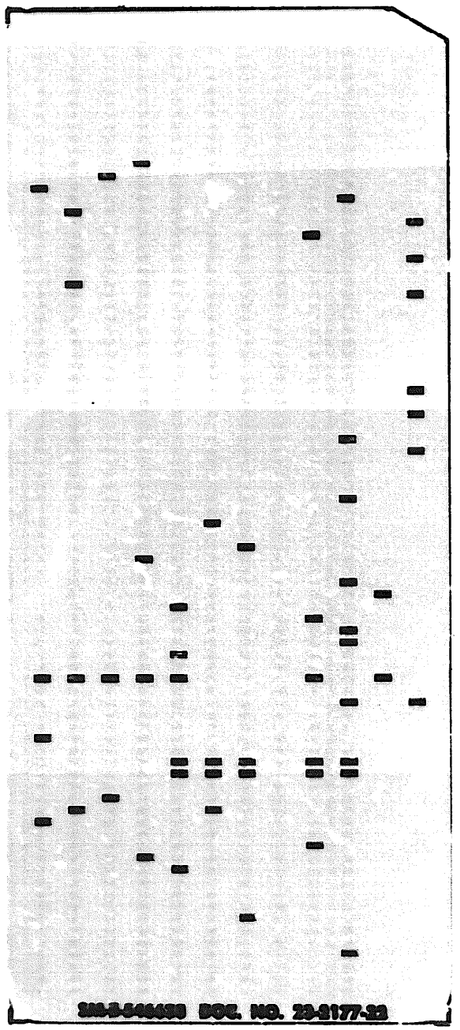
MECHANICAL ASSY — SM-E-546638

POWER INPUT PINS		
	7: THRU Z1(215,247,327 THRU 228	212,216
+4.5 VDC	6	6
GRD	1	183

P.C. Assembly SM-E-546638

P.C. Logic SM-E-546637

Doc. No. 23-2177-22



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO-NO-GO TESTED FIRST.

4 JUMPER ACROSS PINS 1 AND GRD ON FLASH ASSIGNMENT PATCH BOARD PRIOR TO TEST.

APPD. JW DATE 7-7-71

TEST LEGEND AS APPLICABLE

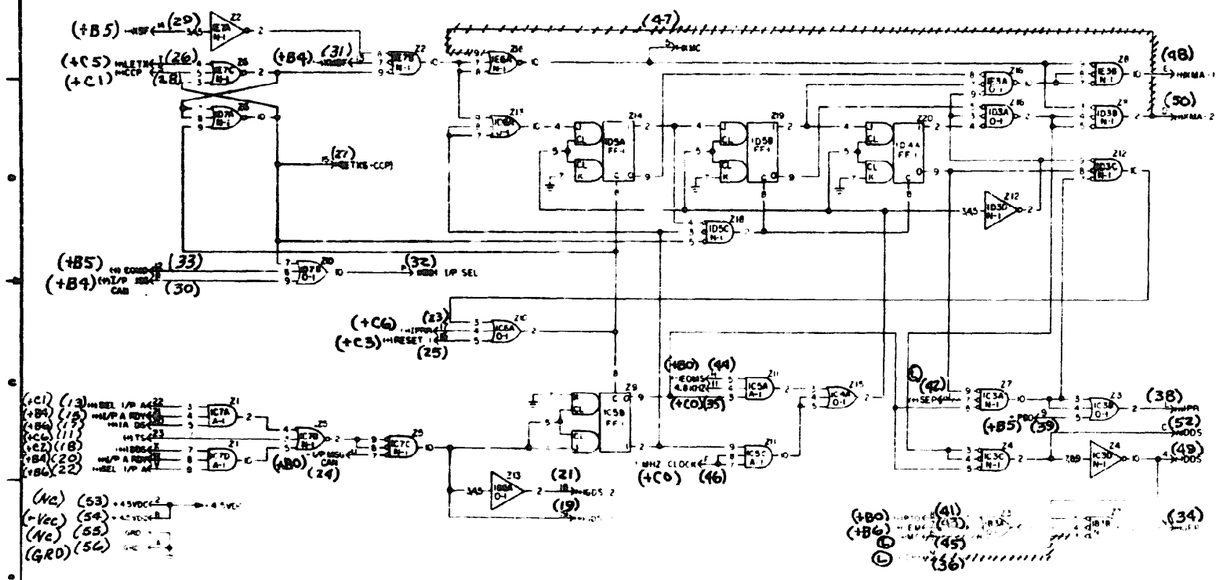
1 ICT PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST

5 ≈≈ INDICATES UNTESTED INPUT/OUTPUT LINES



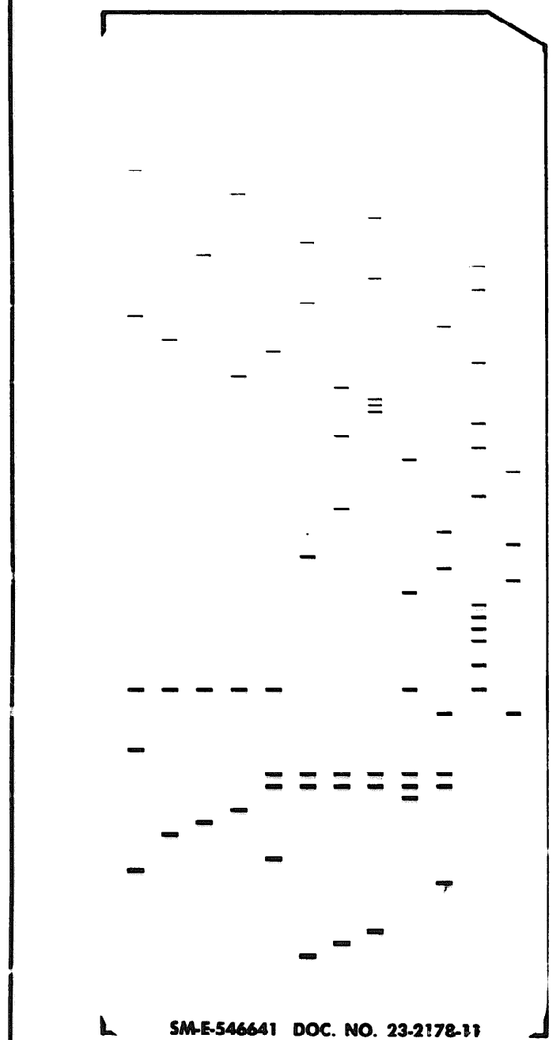
7-2-71

JN

P.C. Assembly SM-E-546641

P.C. Logic SM-E-546640

Doc. No. 23-2178-11



SM-E-546641 DOC. NO. 23-2178-11

TEST PARAMETERS			
+V_{CC}	+4.75	SIG	
-V		LOAD REF V	
+V		CLK	
-V		RST CLR	+OSC

ROW ASSIGNMENT	
10	*B0
1	*C0
2	*B4
3	*B5
4	*B6
5	*B7
6	*C1
7	*C2
8	*C3
9	*C6

INPUT PINS	COL	SIG
35, 46	63	+C0
29* 1*	64	-C1
18*	65	-C2
25*	66	-C3
	67	-C4
26	68	+C5
24* 11*	69	-C6
44, 24, 41	70	+B0
	71	+B1
	72	+B2
	73	+B3
30, 15, 20, 31	74	+B4
29, 33, 39	75	+B5
1, 22, 43	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING	+CO RET
21, 19	A 1 2 3 4 5 6 7 8 B 2 4 6 7 10 11 3 4	
27	A 1 2 3 4 5 6 7 8 9 B 3 4 5 9 8 7 10 # 8	
32	A 1 2 3 4 5 B 3 4 5 9 8	
47	A 1 2 3 4 5 6 B 11 4 7 10 7 6	
(48)	A 1 2 3 B 7 8 10	
(50)	A 1 2 3 B 11 1 3	
(38)	A 1 2 3 4 5 6 7 B 3 8 5 11 9 11 8	
(52) (40)*	A 1 2 3 4 5 B 6 8 9 11 1	
34	A 1 2 3 B 7 8 #	
	A B	
	A B	
	A B	
	A B	
	A B	
	A B	
	A B	
	A B	
	A B	
	A B	
	A B	
	A B	
	A B	

WAVEFORMS

DYNATRONICS TESTAGRAM

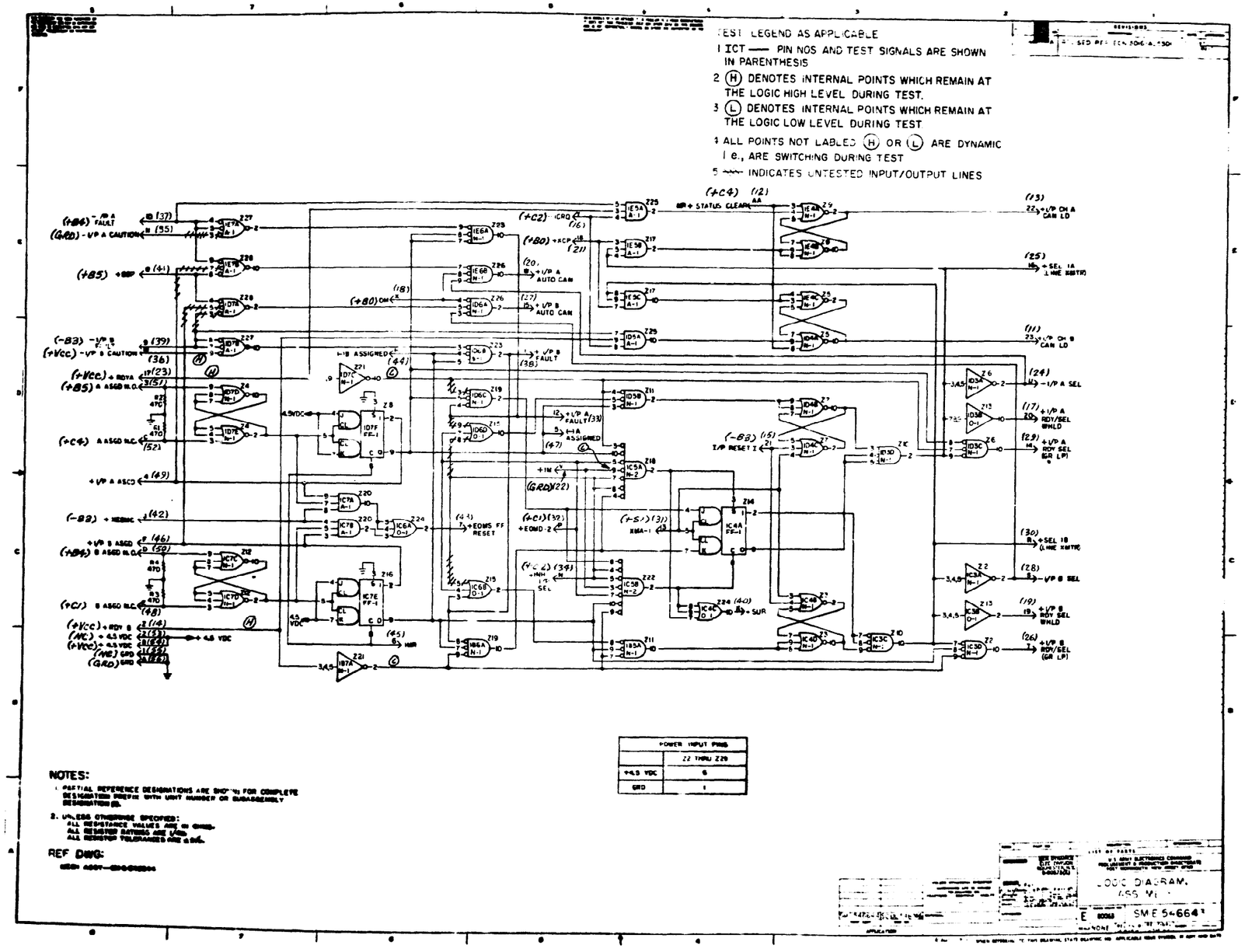
]

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

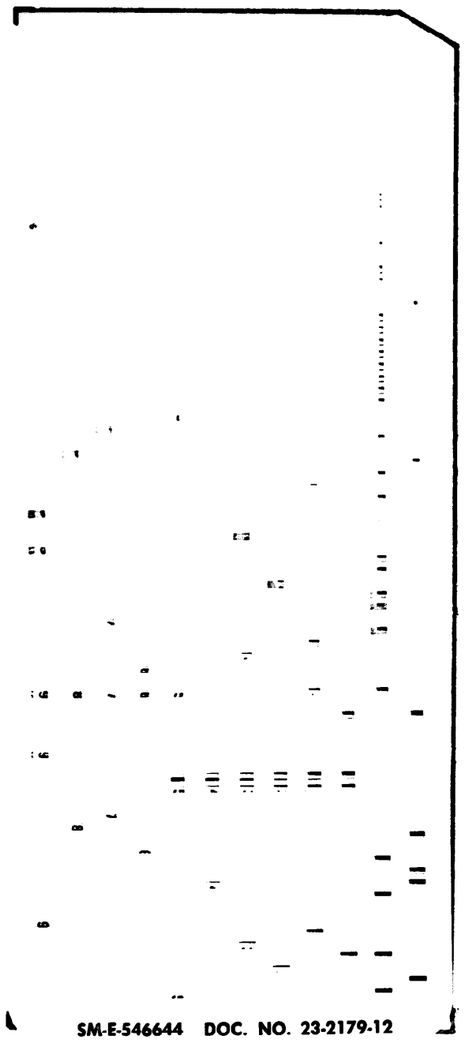
   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

T APPD. JN DATE 7-7-71



P.C. Assembly SM-E-54664

6 4 P.C. Logic SM-E-546643 Doc. No. 23-2179-12



SM-E-546644 DOC. NO. 23-2179-12

TEST PARAMETERS			
V_{CC}	+4.75V	SIG	FREQ. GRD.
-V	—	LOAD AMP V	TP, VCC TP, GRD
+V	—	CLR	1 μ SEC
-V	—	OFF CLR	+OSC

ROW ASSIGNMENT	
10	—
1	+B4
2	+B7
3	+B5
4	+B0
5	+S1
6	+C4
7	+C1
8	+C2
9	-B3

INPUT PINS	COL	SIG
	63	+CO
32*, 45*	64	-C1
16*, 34*	65	-C2
	66	-C3
12*, 52*	67	-C4
	68	+C5
	69	-C6
18, 21	70	+B0
	71	+B1
	72	+B2
15*, 39*, 42*	73	+B3
50	74	+B4
41, 51	75	+B5
	76	+B6
45	77	+B7
	78	+S0
31	79	+S1
	80	+S2
	+CO REF	

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
(29)	A 1 2 3 4 5 6 7
	B 2 7 3 5 11 10 #
47, 49 *	A 1 2 3
	B 2 11 #
17, 25, 24*	A 1 2
	B 3 3
(26)	A 1 2 3 4 5 6 7 8 9
	B 4 6 10 1 3 3 11 8 #
19, 30, 28*	A 1 2 3 4 5 6 7
	B 6 10 NT NT 8 10 #
46, 44*	A 1 2 3
	B 4 3 11
38	A 1 2 3
	B 7 1 3
13	A 1 2 3 4 5
	B 7 7 9 11 #
11	A 1 2 3 4
	B 6 2 10 5
20	A 1 2 3 4 5 6
	B 5 7 9 NT NT 3
27	A 1 2 3 4 5 6 7 8 9 10 11
	B 7 9 NT NT NT NT NT NT NT 3 8
40	A 1 2 3 4 5 6 7 8 9
	B 6 8 10 2 5 NT NT 11 2
48	A 1 2 3 4 5 6 7 8 9
	B 1 3 11 5 10 11 8 10 #
33	A 1 2 3
	B 11 10 #
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B

* BO REF

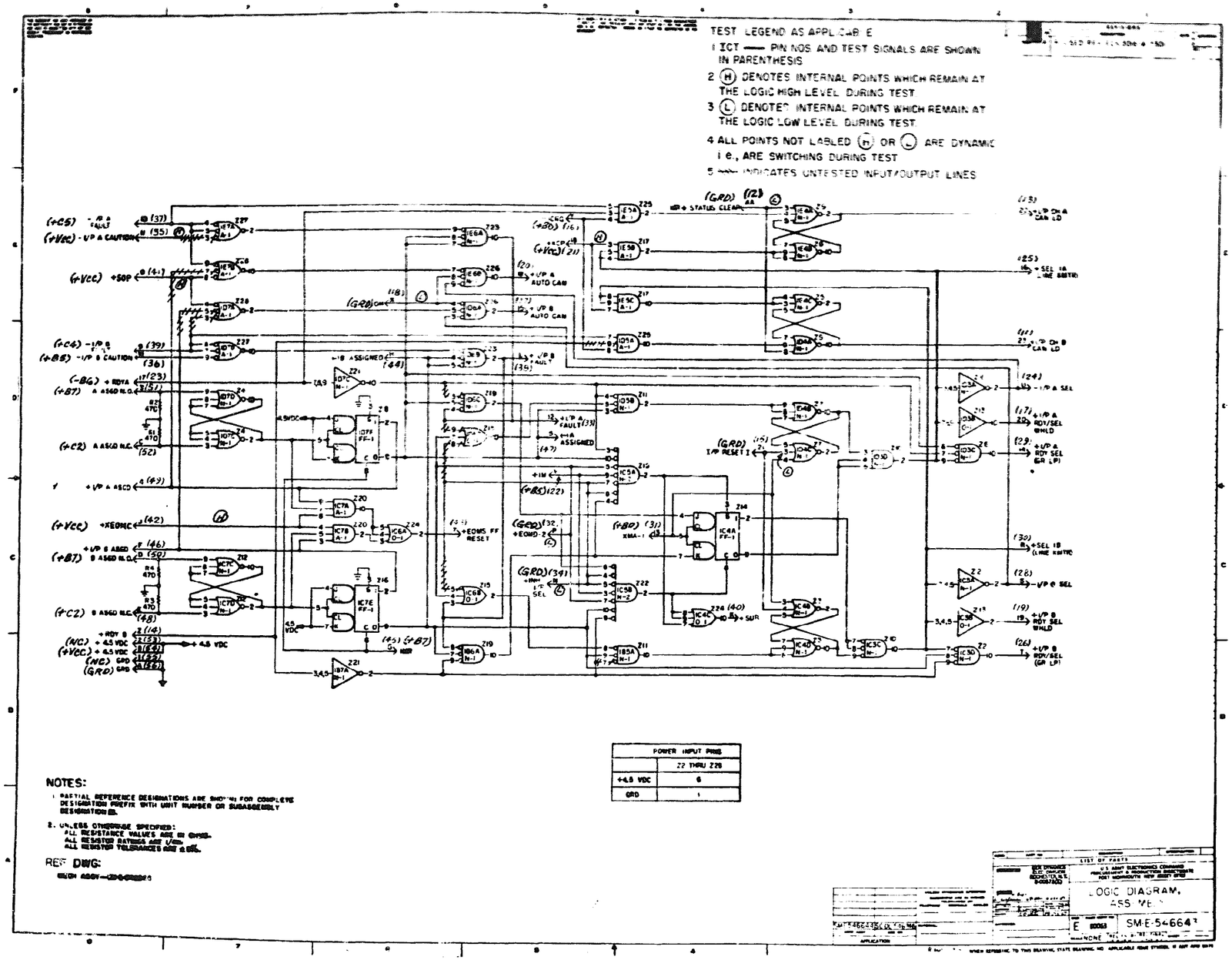
WAVEFORMS — 4 μ SEC

DYNATRONICS TESTAGRAM

NOTES:

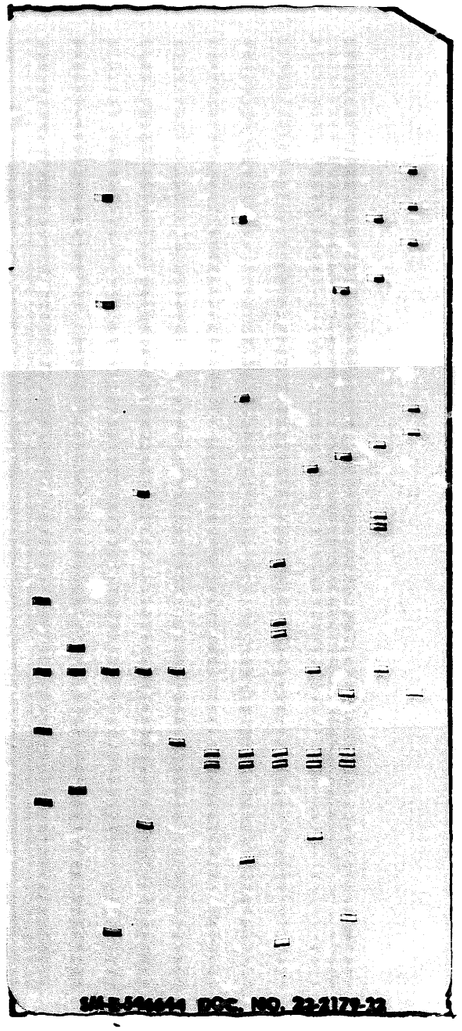
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
5. NT INDICATES NO TEST.



P.C. Assembly SM-E-546644

6 6 P.C. Logic SM-E-546643



TEST PARAMETERS

V_{CC}	+4.75V	SIG V	+VCC, GRD
0V	—	LOAD REF V	[illegible]
0V	—	CLK	1 μs/div
-V	—	BIT CLK	OSC

ROW ASSIGNMENT

10	+B5
1	+C5
2	+B7
3	+B6
4	—
5	—
6	+C4
7	-B6
8	+C1
9	+C2

INPUT PINS	TOL	SIG
	63	+C0
52*	64	-C1
48*	65	-C2
	66	-C3
35*	67	-C4
57	68	+C5
	69	-C6
10, 31	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
22, 56	75	+B5
16*, 33*	76	+B6
45, 50, 51	77	+B7
	78	+S0
	79	+S1
	80	+S2

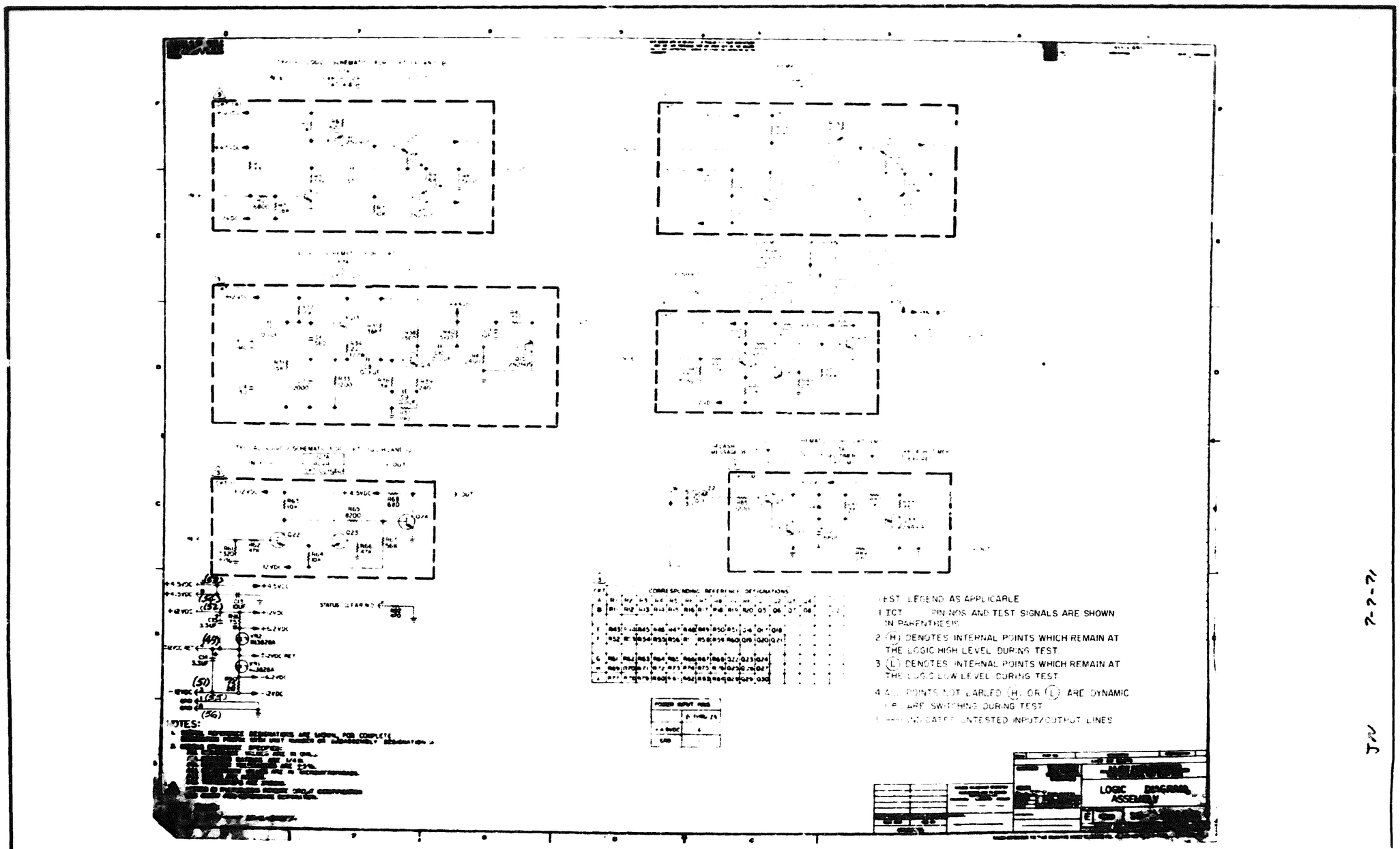
OUTPUT PINS (TEST POINTS)	SWITCH SETTING	+C0 REF
29	A 1 2 3 4 5 6 7 8 9 B 5 9 3 NT NT NT NT 9 7	
13	A 1 2 3 4 5 6 7 8 9 B 4 10 1 11 NT NT NT 11 9	
11	A 1 2 B 3 6	
40	A 1 7 B 4 11	
33	A 1 2 3 B 8 9 2	
26	A 1 2 3 4 B 6 3 5 5	

WAVEFORMS

DYNATRONICS TESTAGRAM

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. NT INDICATES NO TEST.



P.C. Assembly SM-E-546647
P.C. Logic SM-E-546646

TEST PARAMETERS			
Vcc	+4.75	BIG V	2 usec
6V		LOAD	1/4 VCC
+V	12	CLK	32 u sec
-V	12	BIT CLK	+OSC

NOW ASSIGNMENT	
IO	ROUTE PIN 34 TO 15, 76, 78
1	—
2	+12V
3	—
4	-12V
5	GND
6	—
7	+B4
8	+B5
9	+B6

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
(20)(10)(3) 34, 35, 36	A 1 2 3 4 / B 2 1 11 10
11, 16	A 1 7 3 4 / B 2 1 5 4
18, 21 ▷	A 1 2 3 4 / B 2 11 9 7

INPUT PINS	COL	SIG
	63	+CO
	64	C
	65	+C2
	66	+C3
	67	+C4
	68	+C5
	69	+C6
	70	+B7
	71	+B1
	72	+B2
	73	+B3
13, 37, 48, 56	74	+B4
14, 19	75	+B5
17	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+CO REF

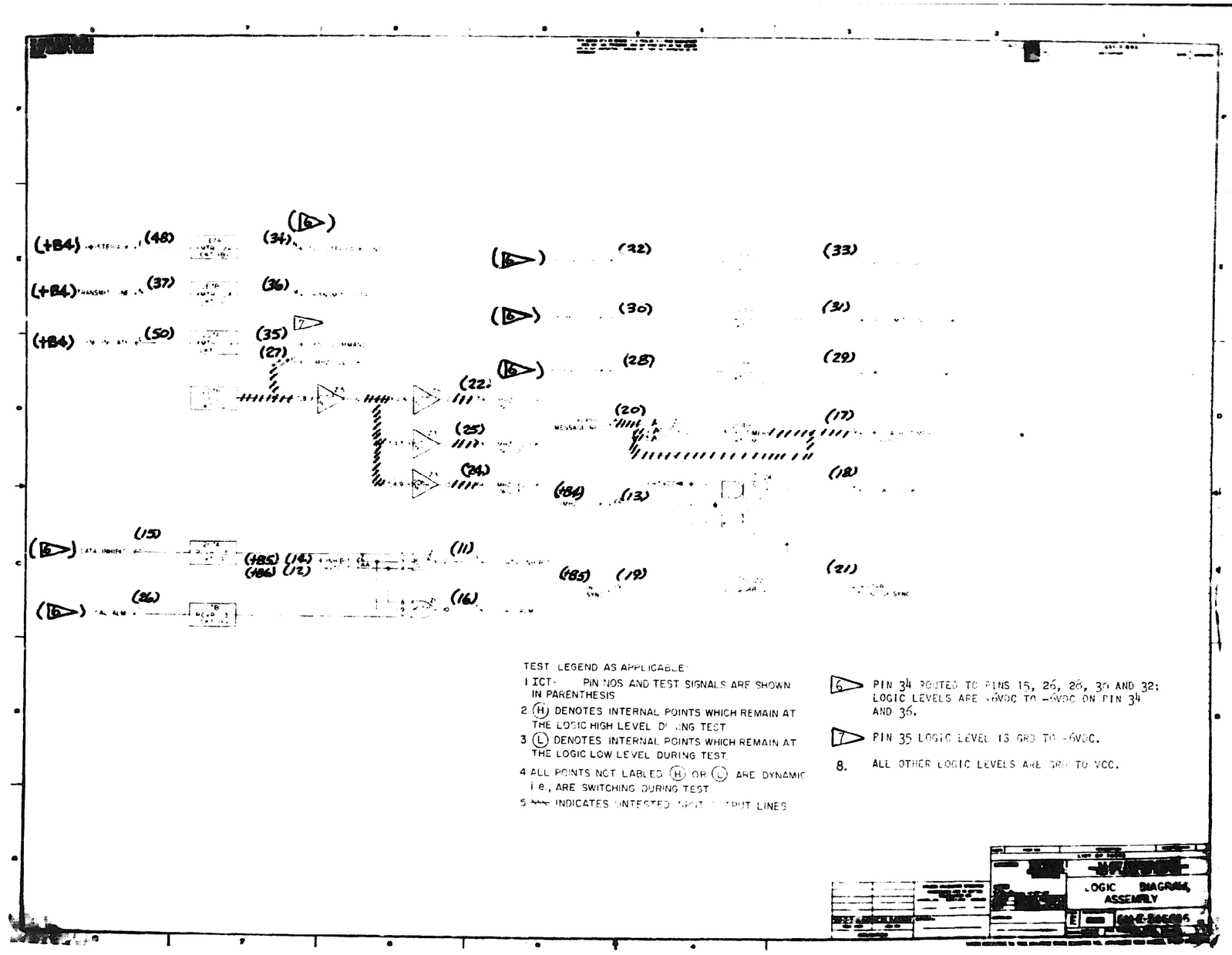
WAVEFORMS — ← → 128 u sec — DYNATRONICS YESTAGRAM

NOTES:

1. ▷ PIN 18 OUTPUT CAN BE NORMAL OR INVERTED.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. SIGNAL LEVELS ON PINS 34 AND 36 ARE -6V TO +6V.
5. SIGNAL LEVELS ON PIN 35 ARE OV AND +6V.
6. ALL OTHER SIGNALS ARE OV TO +4.5V.

SM-E-546647 DOC. NO. 23-2180-11

GOVT APPD. JN DATE 7-7-71



TEST LEGEND AS APPLICABLE:

1 ICT- PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.

5 ~~~ INDICATES UNTESTED INPUT OUTPUT LINES

6 PIN 34 ROUTED TO PINS 15, 26, 28, 30 AND 32; LOGIC LEVELS ARE +6VDC TO -6VDC ON PIN 34 AND 36.

7 PIN 35 LOGIC LEVEL IS GRD TO -6VDC.

8. ALL OTHER LOGIC LEVELS ARE GRD TO VCC.

2-2-71

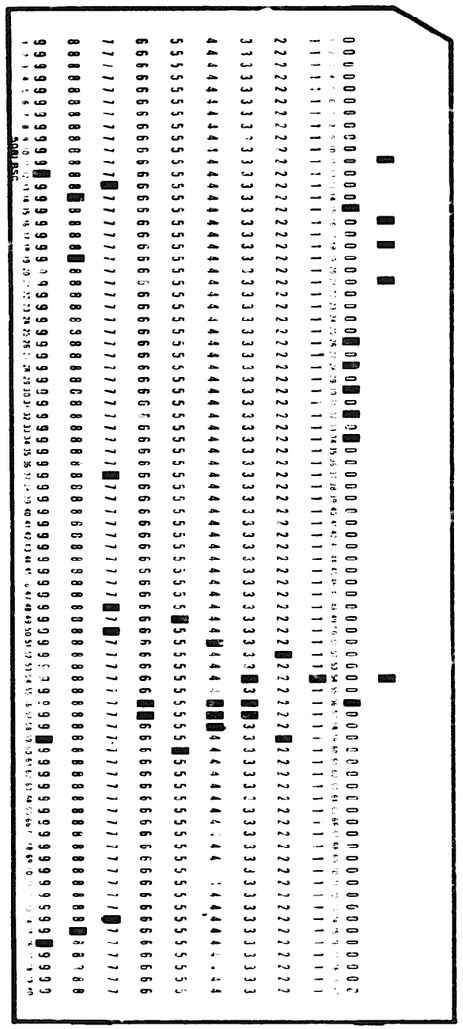
JW

7 0

P.C. Assembly SM-E-516647

P.C. Logic SM-E-516646

Dwg. No. 23-4180-1

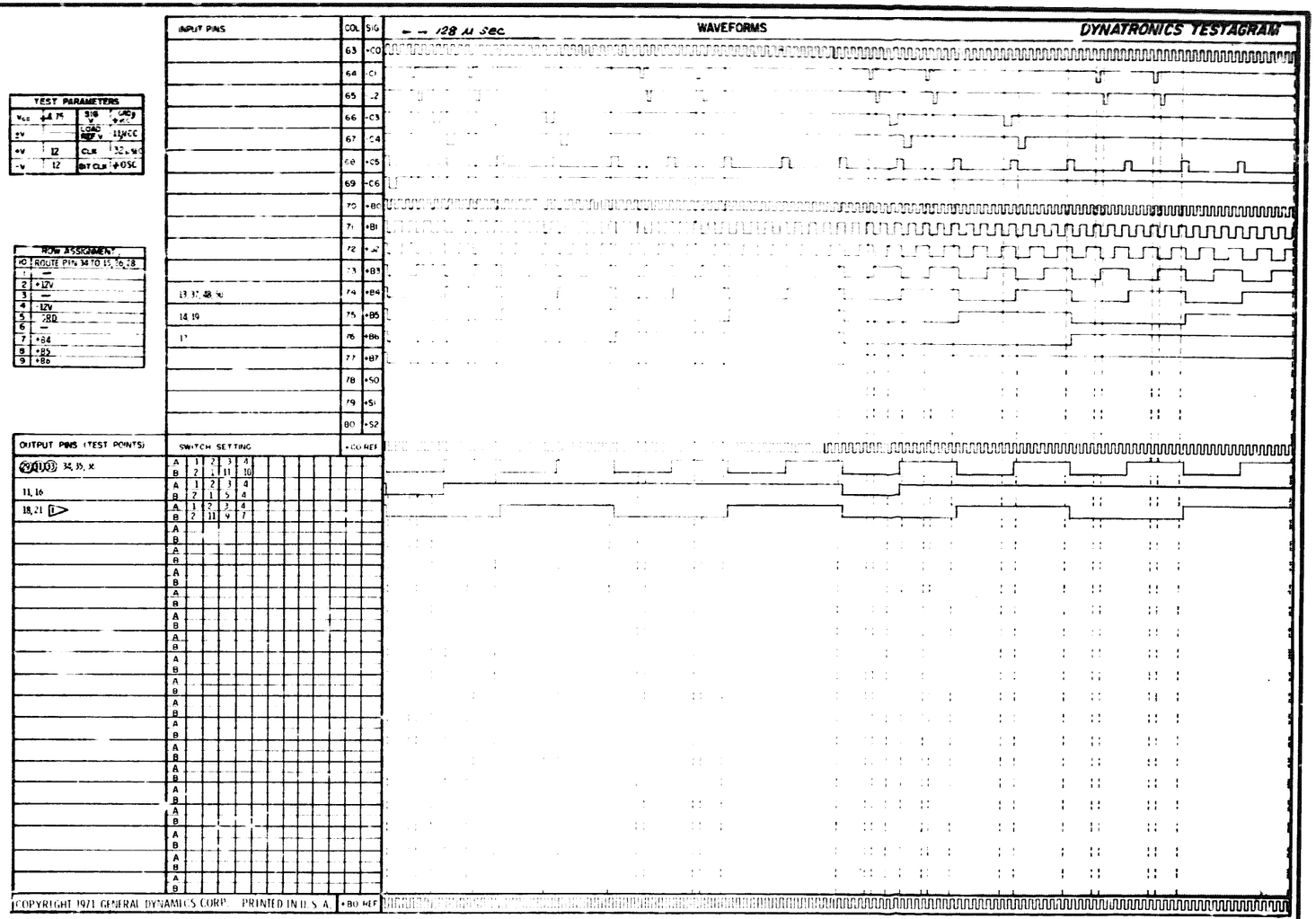


TEST PARAMETERS			
V_{CC} +4.75		SIG G	GRD +VCC
0V		LOAD REF V	1/2VCC
+V	12	CLK	32.4 KC
-V	12	BIT CLR	+OSC

ROW ASSIGNMENT	
NO	ROUTE PIN 34 TO 35, 36, 38
1	—
2	+12V
3	—
4	-12V
5	GRD
6	—
7	+B4
8	+B5
9	+B6

INPUT PINS	COL	SIG
	63	+C0
	64	C1
	65	C2
	66	C3
	67	C4
	68	C5
	69	C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
13, 37, 48, 50	74	+B4
14, 19	75	+B5
17	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
(20)(40)(60) 34, 35, 36	+CO REF
11, 16	
18, 21 ▷	



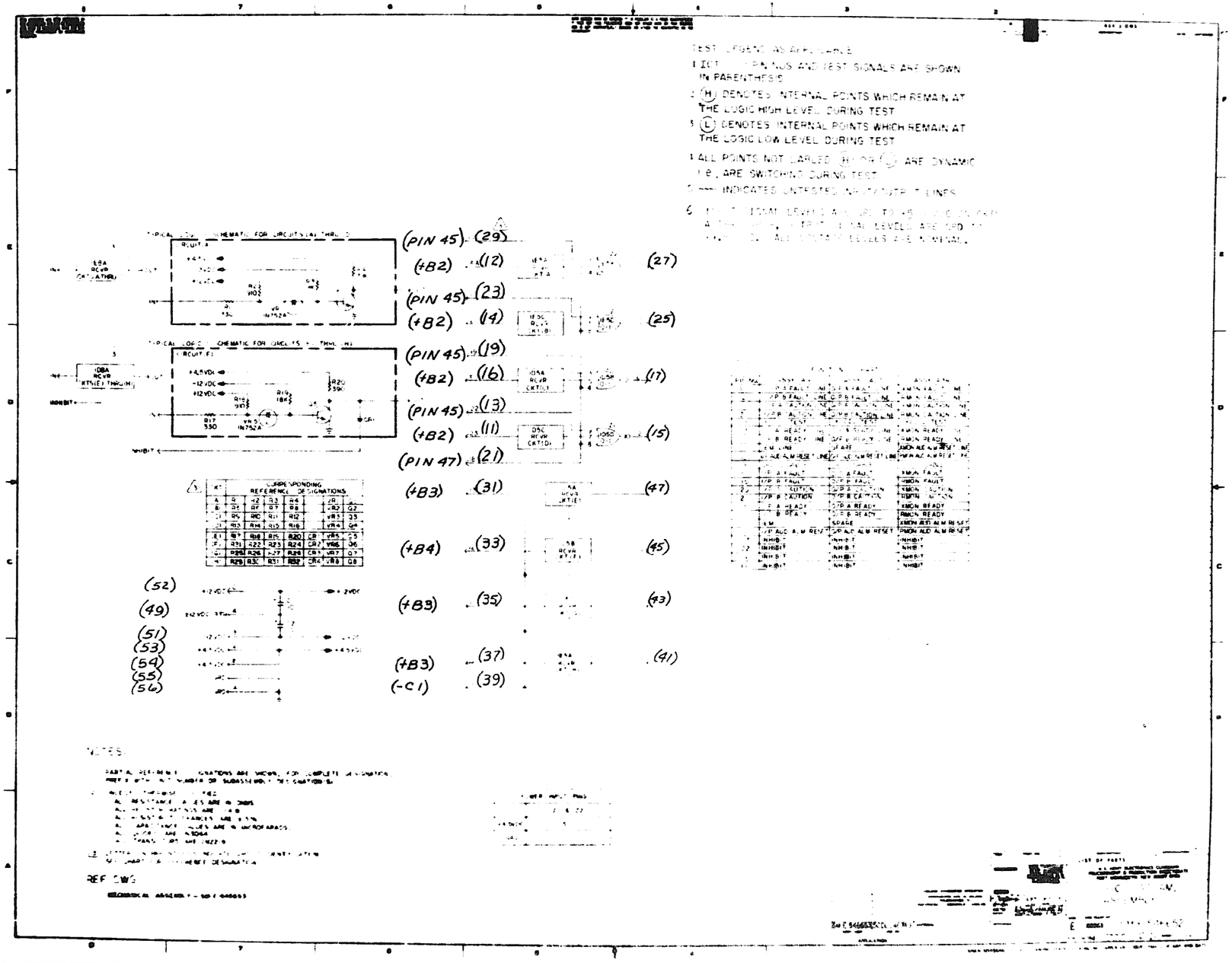
NOTES:

1. PIN 18 OUTPUT CAN BE NORMAL OR INVERTED.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. SIGNAL LEVELS ON PINS 34 AND 36 ARE -6V TO +6V.
5. SIGNAL LEVELS ON PIN 35 ARE OV AND +6V.
6. ALL OTHER SIGNALS ARE OV TO +4.5V.

JN 7-7-71

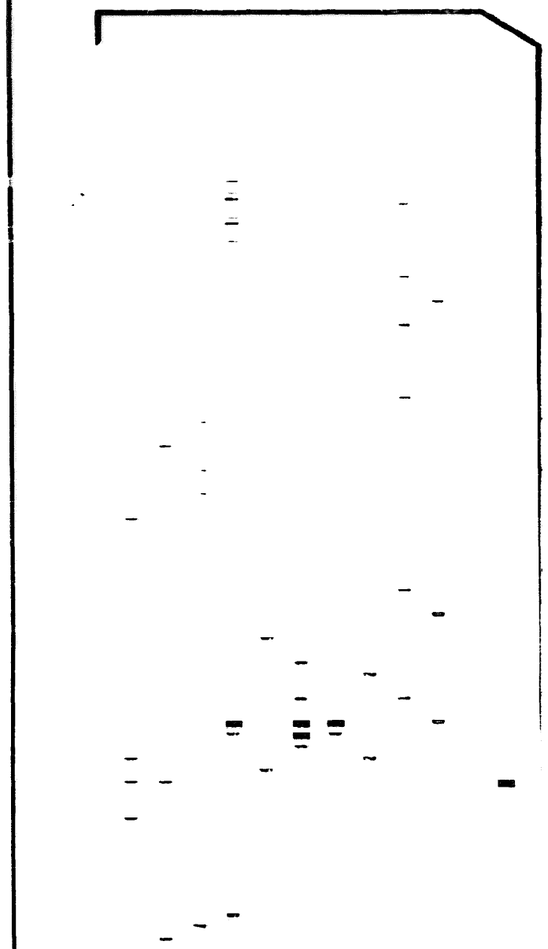
Doc. No. 23- 2180-11

P.C. Assembly SM-E-546647
P.C. Logic SM-E-546646



P.C. Assembly SM-E-54bb53

P.C. Logic SM-E-54bb52 Dwg. No. 25-2181-11



SM-E-546653 DOC. NO. 23-2181-11

GOVT APPD. JN DATE 7-7-71

TEST PARAMETERS

V_{CC}	+4.75	SIG V	+3.8 GRD
+V	+5.8	LOAD REF'n	—
+V	12	CLK	2 μ SEC
-V	12	INT CLK	↑ 05C

ROW ASSIGNMENT

10	ROUTE PIN 47 TO 21
1	ROUTE PIN 45 TO 13, 19, 23, 29
2	+12V
3	—
4	-12V
5	GRD
6	+B2
7	+B3
8	+B4
9	-C1

INPUT PINS		SIG
	63	+C0
62	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	-C5
	69	-C6
	70	+B7
	71	+B1
12, 14, 16, 18	72	+B2
31, 35, 37	73	+B3
33	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS) — SWITCH SETTING — +80 REF

41, 43, 47

15 17 & 25 27

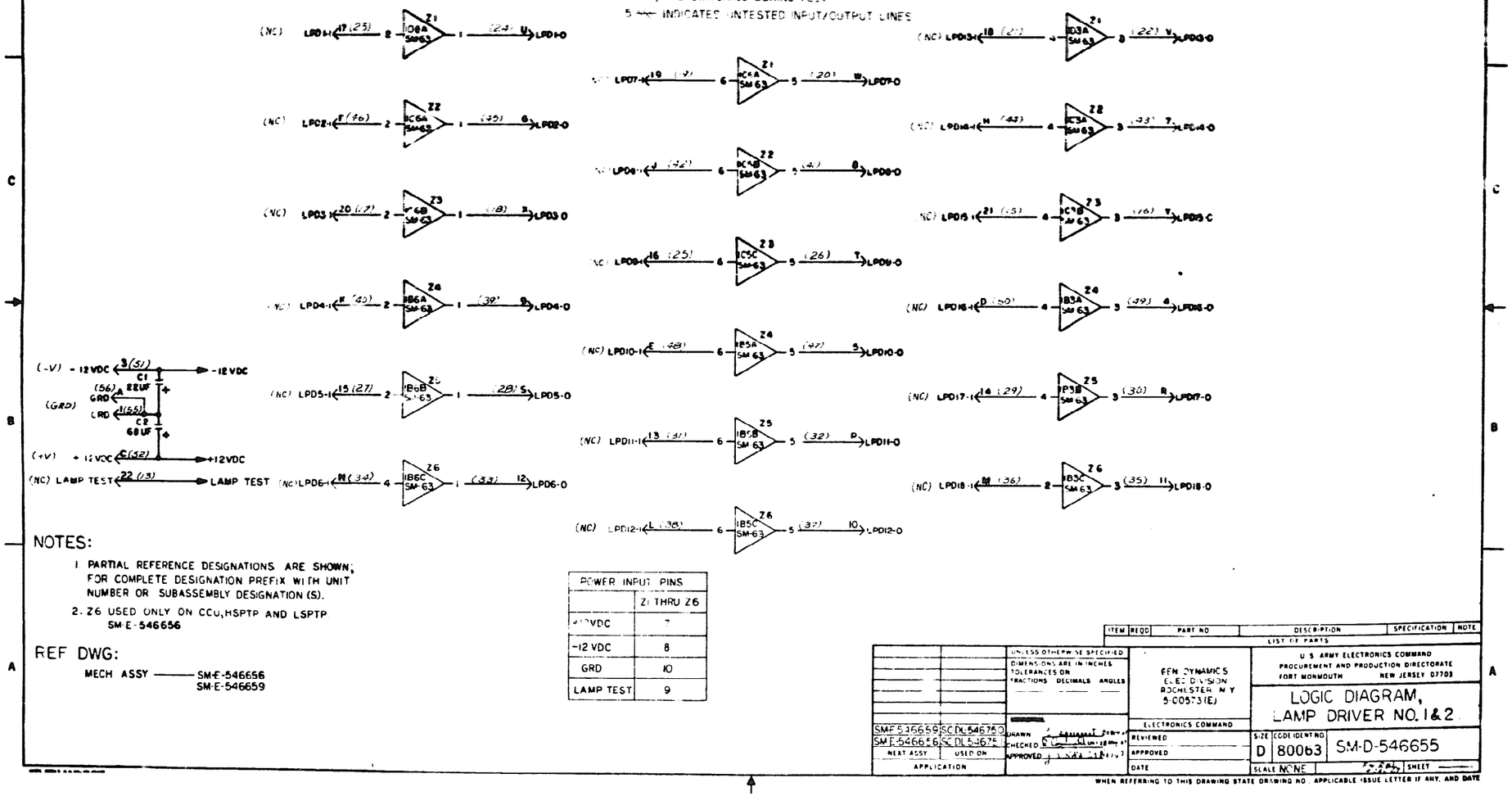
45

NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
3. REDUCED SIGNAL SWINGS AT THESE POINTS ARE CAUSED BY THE FORWARD VOLTAGE DROP ACROSS THE DIODE IN THE INHIBIT INPUT.

NOTE
DATA MARKED WITH AN ASTERISK (*) IS PECULIAR TO A PD OR MANUFACTURER IT DOES NOT TAKE PRECEDENCE OVER ANY OTHER DATA ON THIS DRAWING AND IS NOT CONTRACTUALLY BINDING ON EITHER THE CONTRACTOR OR THE GOVERNMENT.

1 ICT—— P/N NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST
5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S).
2. Z6 USED ONLY ON CCU, HSPTP AND LSPTP SM-E-546656

REF DWG:

MECH ASSY —— SM-E-546656
SM-E-546659

POWER INPUT PINS	
	Z1 THRU Z6
+12 VDC	7
-12 VDC	8
GRD	10
LAMP TEST	9

ITEM	REQD	PART NO	DESCRIPTION	SPECIFICATION	NOTE

LIST OF PARTS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES

SMF 546656 SCDL 546753
SMF 546656 SCDL 546754
NEXT ASSY USED ON
APPLICATION

DRAWN
CHECKED
APPROVED

GEN DYNAMICS
ELEC DIVISION
ROCHESTER N Y
5-05731(E)

ELECTRONICS COMMAND
REVIEWED
APPROVED
DATE

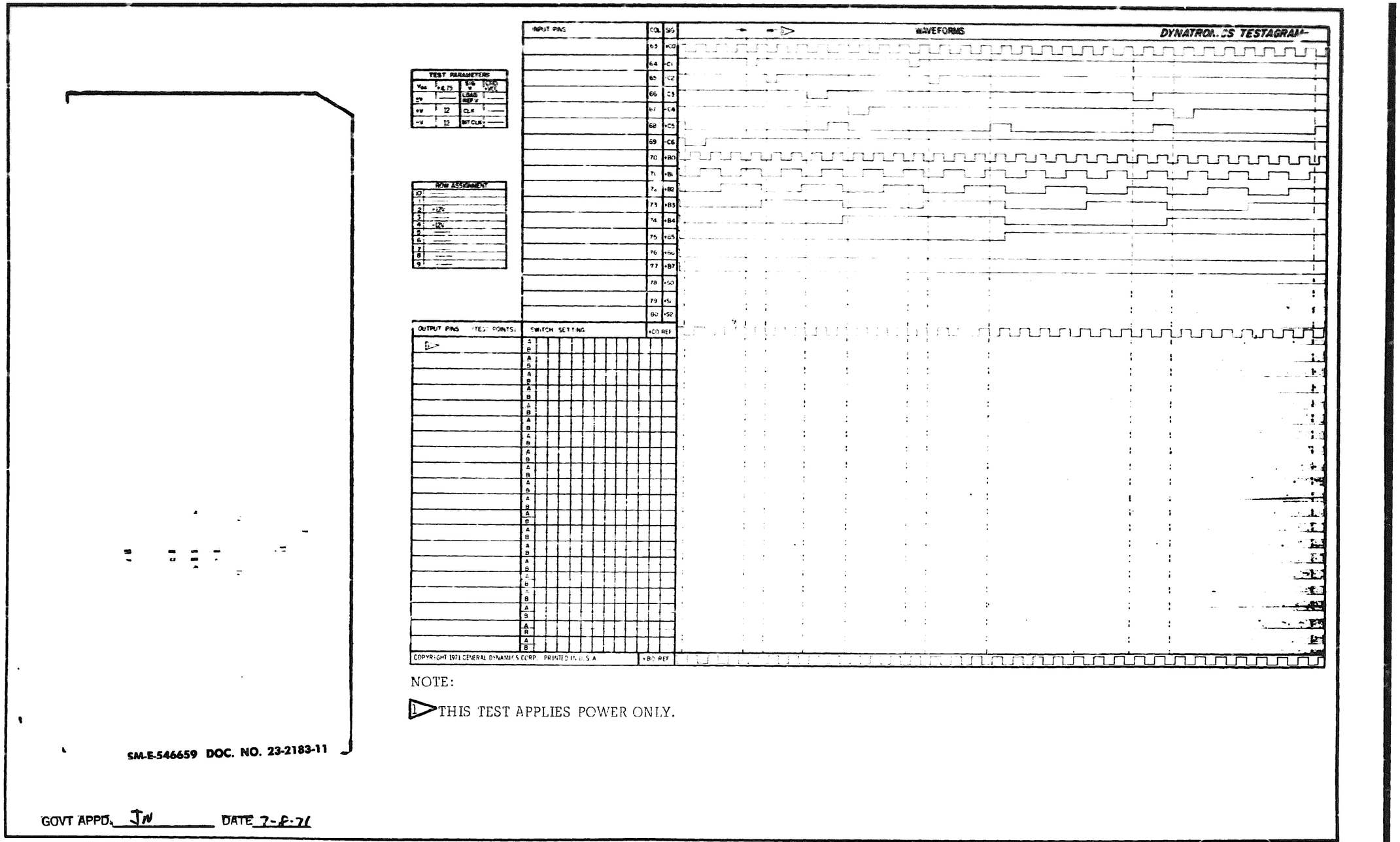
U S ARMY ELECTRONICS COMMAND
PROCUREMENT AND PRODUCTION DIRECTORATE
FORT MONMOUTH NEW JERSEY 07703

LOGIC DIAGRAM,
LAMP DRIVER NO. 1 & 2

SIZE D | CODE IDENT NO 80063 | SM-D-546655
SCALE NONE | SHEET

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE ISSUE LETTER IF ANY, AND DATE

P.C. Assembly SM-E-546656 and SM-E-546659
P.C. Logic SM-D-5466455



NOTE:

1. THIS TEST APPLIES POWER ONLY.

SM-E-546659 DOC. NO. 23-2183-11

GOVT APPD. JN DATE 7-8-71

TEST LEGEND AS APPLICABLE

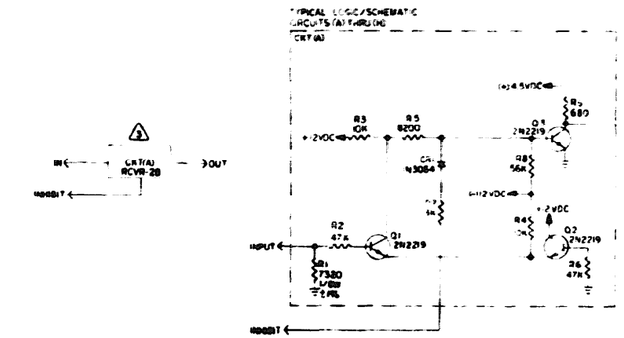
1 ICT ... PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.

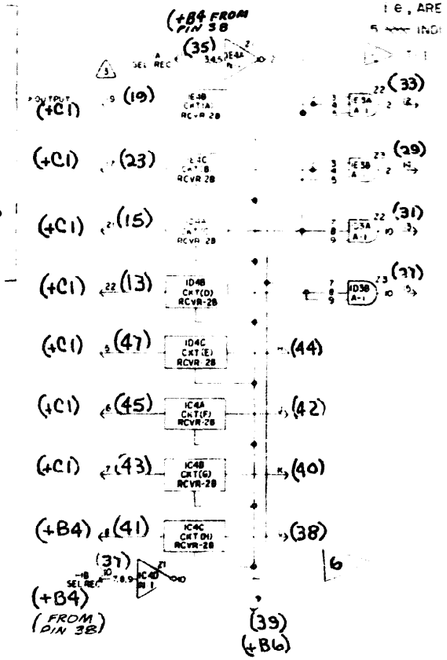
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST.

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES.



(3)

CORRESPONDING REFERENCE DESIGNATION																	
CKT (A)	CR1	Q1	Q2	Q3	R1	R2	R3	R4	R5	R6	R7	R8	R9				
CKT (B)	CR2	Q4	Q5	Q6	R10	R11	R12	R13	R14	R15	R16	R17	R18				
CKT (C)	CR3	Q7	Q8	Q9	R19	R20	R21	R22	R23	R24	R25	R26	R27				
CKT (D)	CR4	Q10	Q11	Q12	R28	R29	R30	R31	R32	R33	R34	R35	R36				
CKT (E)	CR5	Q13	Q14	Q15	R37	R38	R39	R40	R41	R42	R43	R44	R45				
CKT (F)	CR6	Q16	Q17	Q18	R46	R47	R48	R49	R50	R51	R52	R53	R54				
CKT (G)	CR7	Q19	Q20	Q21	R55	R56	R57	R58	R59	R60	R61	R62	R63				
CKT (H)	CR8	Q22	Q23	Q24	R64	R65	R66	R67	R68	R69	R70	R71	R72				



FUNCTION CHART	
PIN NO.	ASSY A95
9	O/P A DATA REQ
12	(+) O/P A DATA REQ
17	O/P B DATA REQ
14	(+) O/P B DATA REQ
21	O/P A START BLOCK
18	(+) O/P A FIRST DATA REQ
22	O/P B START BLOCK
15	(+) O/P B FIRST DATA REQ
5	XMON DATA REQ
H	(+) XMON DATA REQ
6	RMON DATA REQ
J	(+) RMON DATA REQ
7	XMON START BLOCK
K	(+) XMON FIRST DATA REQ
8	RMON START REQ
L	(+) RMON FIRST DATA REQ
9	(+) CCU TEST

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S).
2. UNLESS OTHERWISE SPECIFIED.
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL RESISTOR TOLERANCES ARE ±5%.
   ALL RESISTOR RATINGS 1/4W.

(3) LETTERS IN PARENTHESIS INDICATE CIRCUIT IDENTIFICATION. SEE CHART FOR REFERENCE DESIGNATIONS.

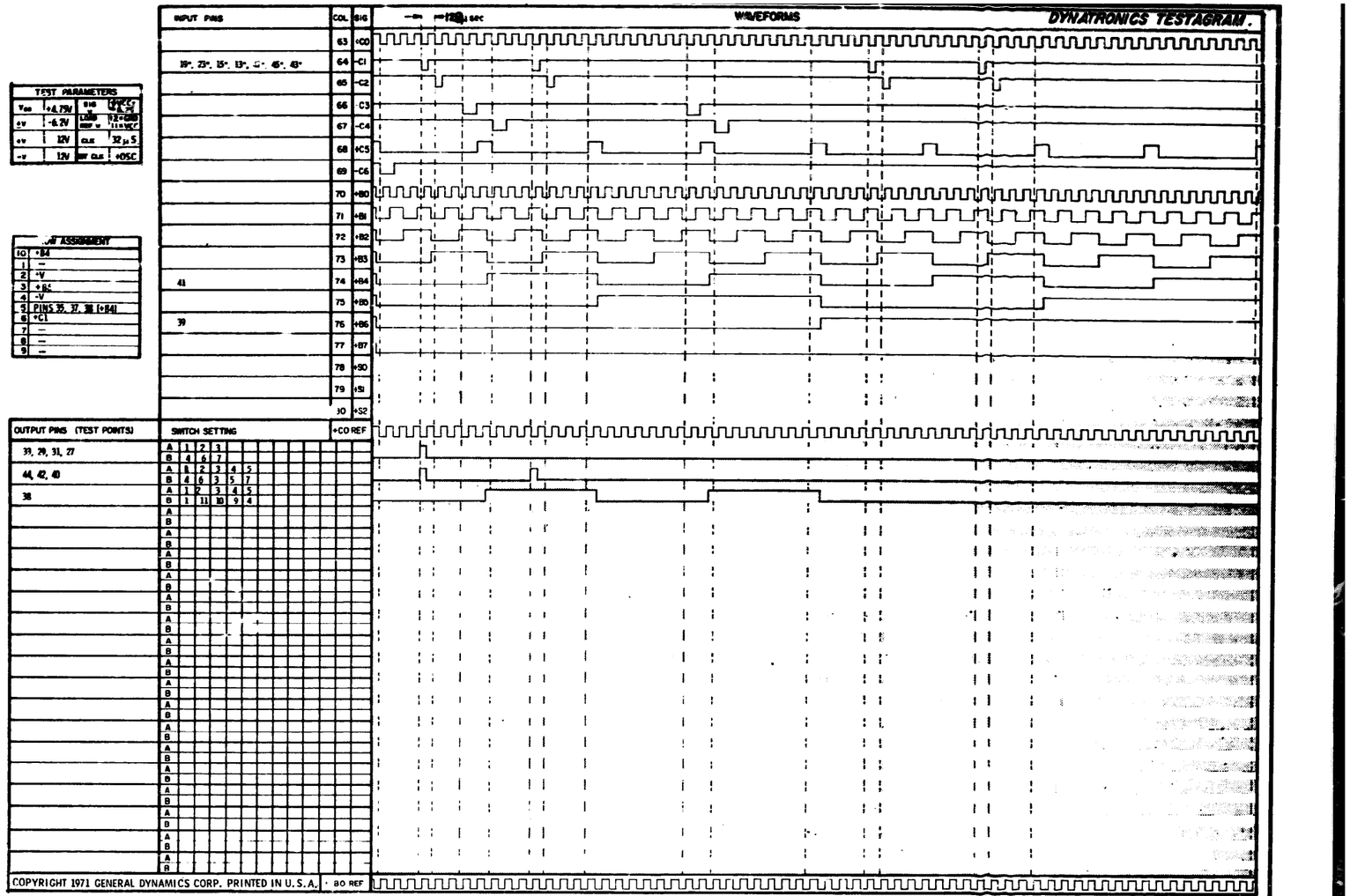
REF DWG:
MECH ASSY —— SM-E-546642

LOGIC DIAGRAM, ASSEMBLY

SM-E-546661

P.C. Assembly SM-E-546662

7 6 P.C. Logic SM-E-546661 Doc. No. 23-2184-11

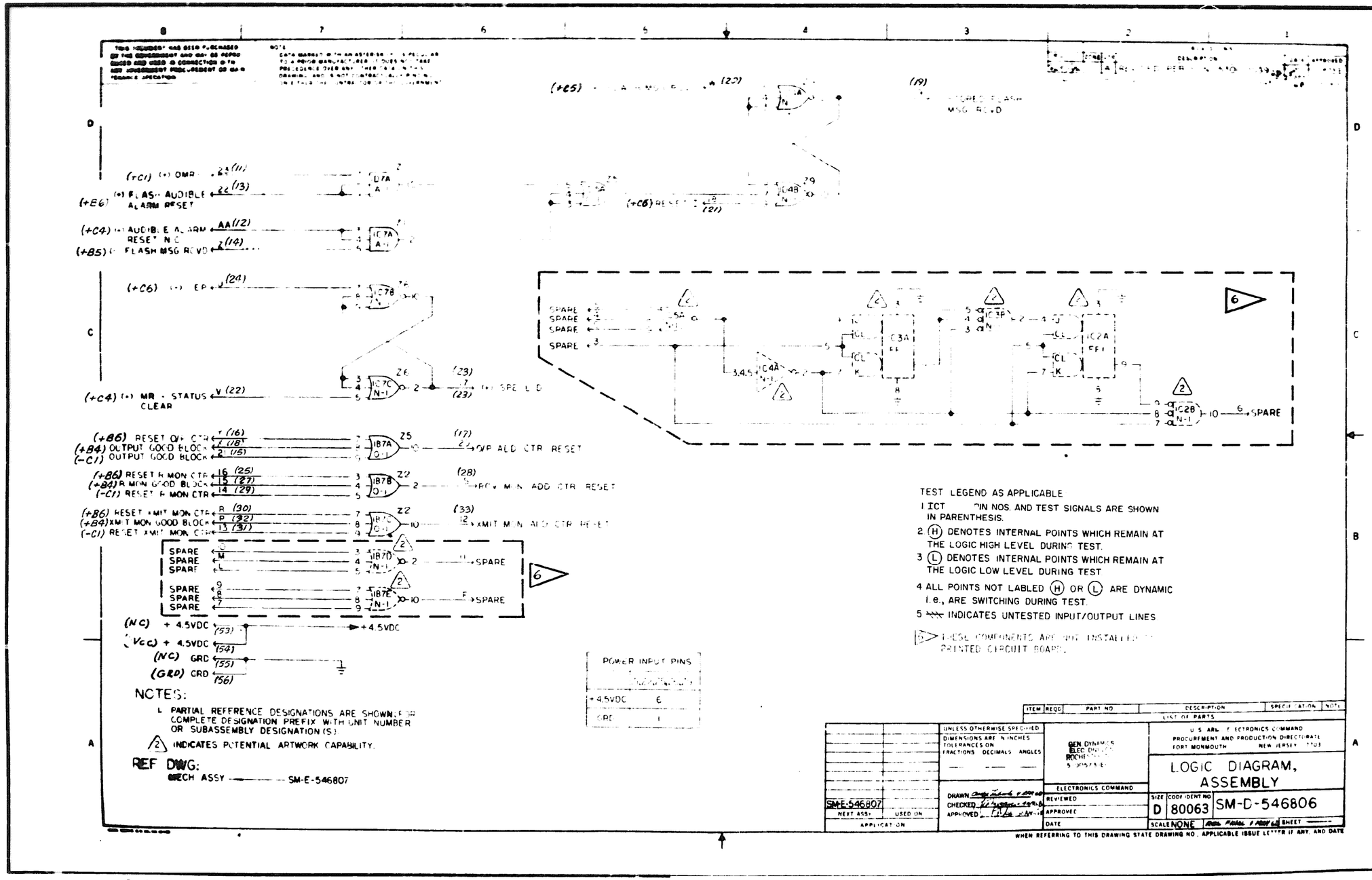


NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

SM-E-546662 DOC. NO. 23-2184-11

GOVT APPD. JN DATE 7-7-71



P.C. Assembly SM-E-546807

P.C. Logic SM-E-546806

Dwg. No. 23-2185-11

TEST PARAMETERS			
V_{CC}	+4.75V	SW1 V	SPEC 3 GRD
+V	—	LOAD REF V	12 = GRD 11 = VCC
∅V	—	C_LK	$T_{\mu S}$
-V	—	ENT CLK	+OSC

ROW ASSIGNMENT	
10	-C1
1	+B4
2	+B5
3	+B6
4	+C5
5	—
6	+C1
7	+C4
8	+C6
9	—

INPUT PINS	COL	SIG
	63	+C0
11*, 15, 29, 31	64	-C1
	65	-C2
	66	-C3
12*, 22*	67	-C4
20	68	+C5
24 21*	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
18, 27, 37	74	+B4
↓	75	+B5
13 16, 25, 30	77	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+C0 REF

WAVEFORMS — DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS)	SWITCH SETTING	1	2	3	4	5	6	7	8
19	A	3	9	11	6	11	5	10	4
	B								
23	A	1	2	3					
	B	3	2	#*					
17, 28, 33	A	1	2	3					
	B	4	6	7					
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								
	A								
	B								

 • B0 REF

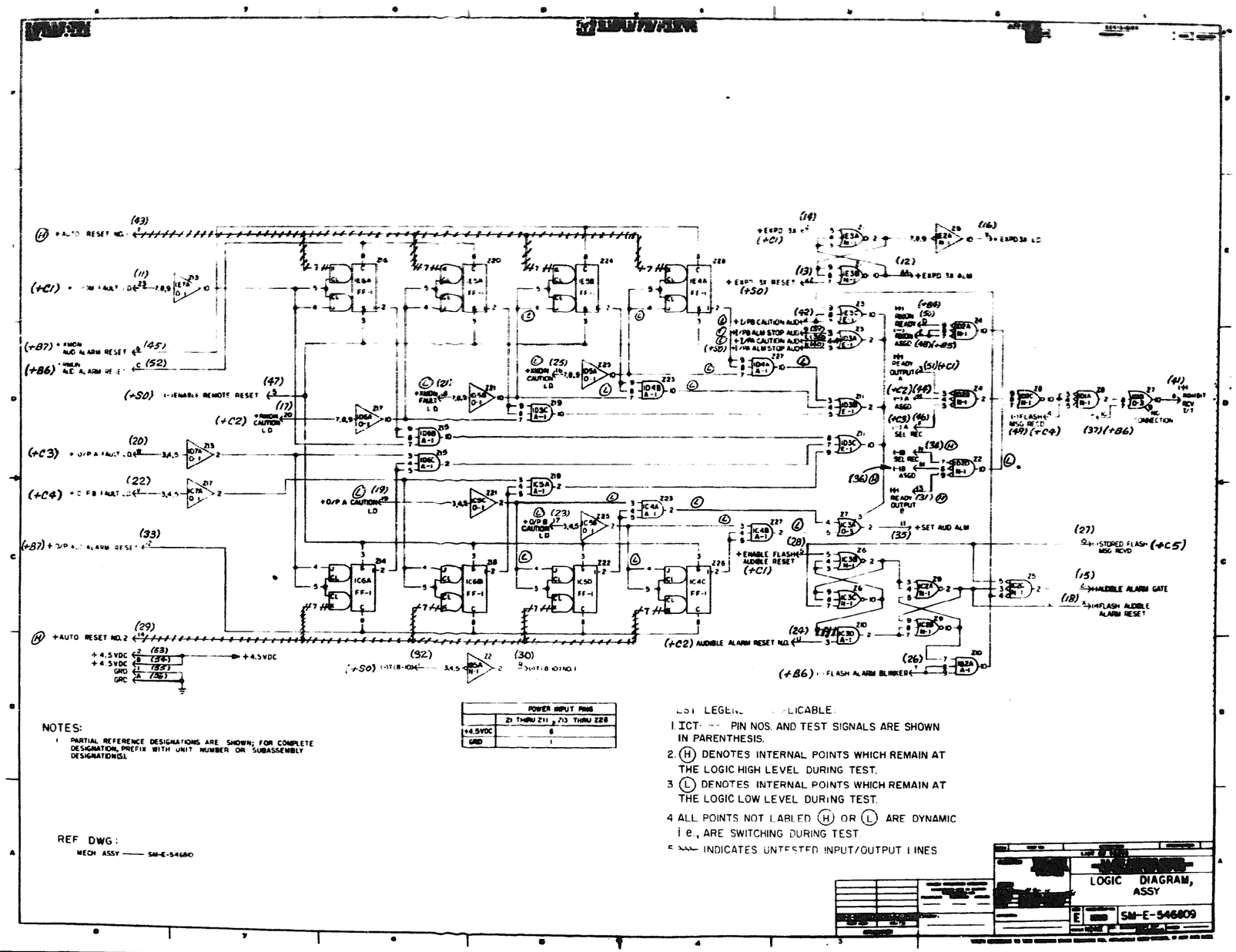
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.

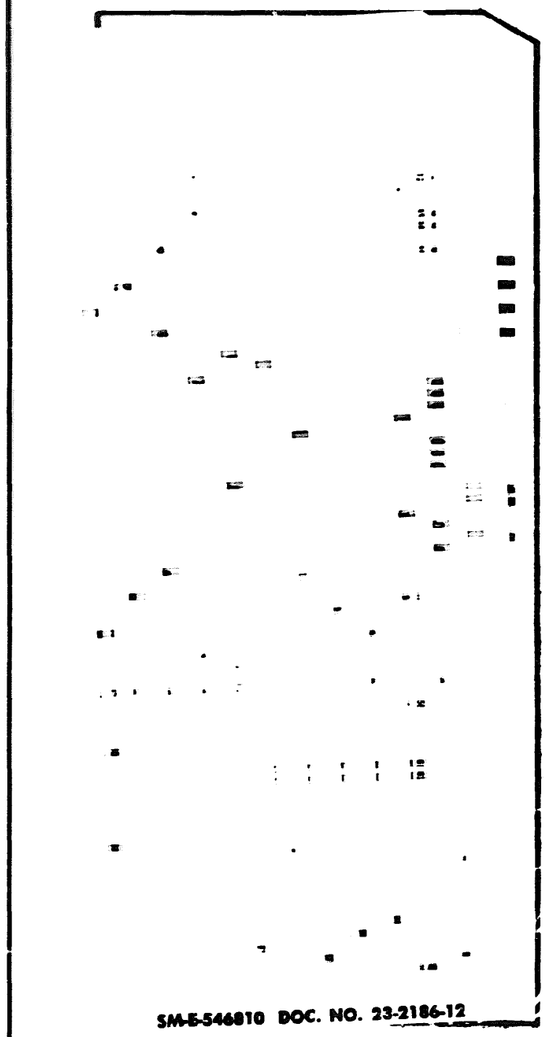
SM-E-546807 DOC. NO. 23-2185-11

GOVT APPD. JN DATE 7-7-71



P.C. Assembly SM-E-546810

8 0 P.C. Logic SM-E-546809 Doc. No. 23-2186-12



SM-E-546810 DOC. NO. 23-2186-12

GOVT APPD. JN DATE 7-7-71

TEST PARAMETERS

V_{CC}	+4.75V	SYS CLK	10 MHz CRYSTAL
-5V	—	LOAD REF. V	2.380 VDC
+V	—	CLK	1 μ SEC
-V	—	INT CLR	+OSC

ROW ASSIGNMENT

10	+S0
1	+S2
2	+S5
3	+S7
4	+C5
5	+S6
6	+C1
7	+C2
8	+C3
9	+C4

OUTPUT PINS (TEST POINTS)

35, 30, 16, 12, 41, 15, 18

INPUT PINS

	COL	SIG
	63	+C0
11*, 14*, 51*, 28*	64	-C1
17*, 44*, 24*	65	-C2
20*, 46*	66	-C3
22*, 49*	67	-C4
27	68	+C5
	69	-C6
	70	+S0
	71	+S1
	72	+S2
	73	+S3
50	74	+S4
48	75	+S5
37, 52, 26	76	+S6
33, 45	77	+S7
47, 32, 13, 40	78	+S0
	79	+S1
	80	+S2

SWITCH SETTING

	1	2	3	4	5	6	7	8	9	10	11	12
A												
B	2	3	7	4	6	8	10	5	9	2	6	9
A	1	2	3									
B	3	7	8									
A	1	2	3									
B	5	4	4									
A	1	2	3	4	5	6	7	8	9	10	11	
B	2	6	3	5	7	9	3	7	11	4	5	
A	1	2	3	4	5	6	7	8	9			
B	3	8	2	7	1	7	11	6	6			
A	1	2	3									
B	8	9	7									
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												

WAVEFORMS — DYNATRONICS TESTAGRAM

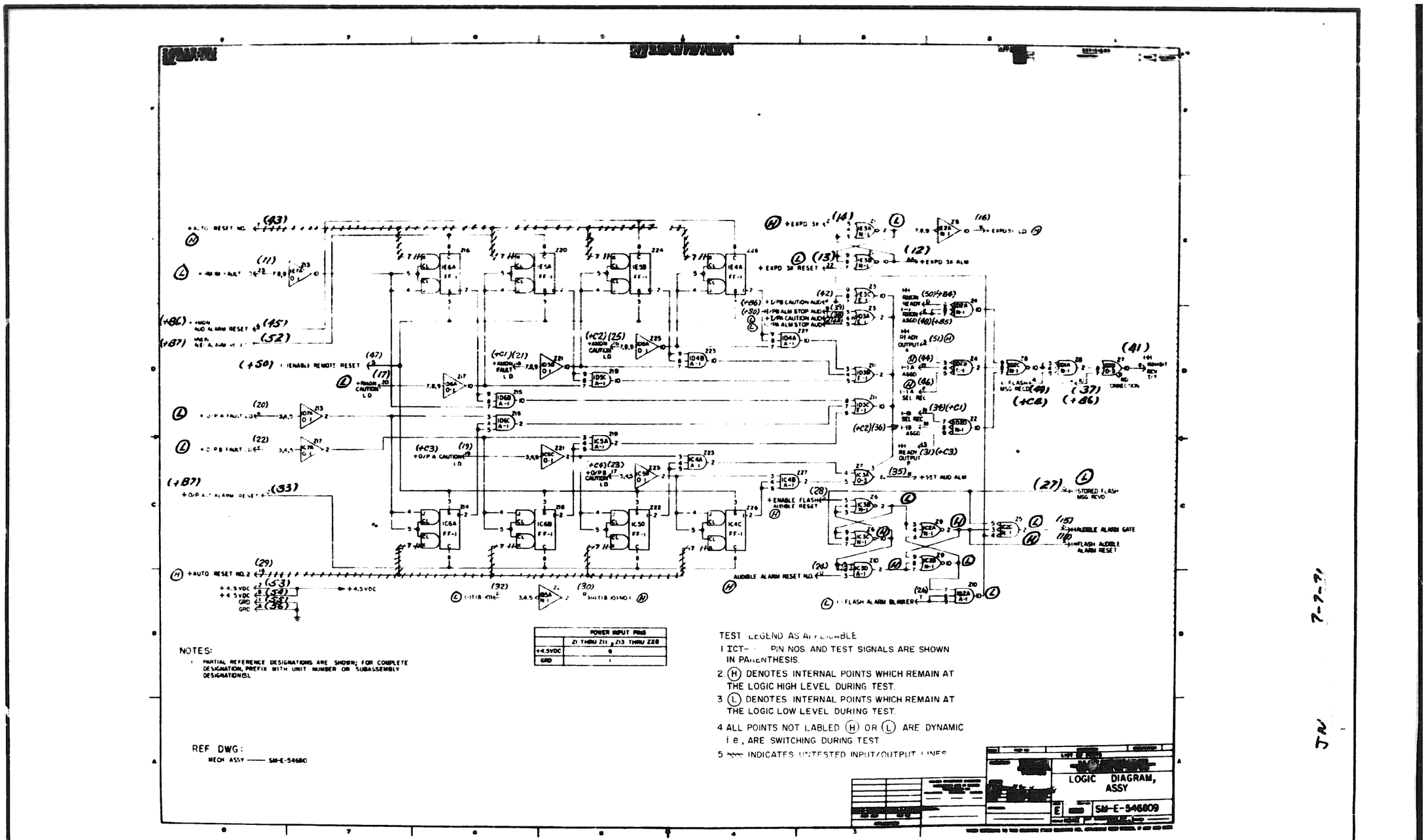
+C0 REF

+B0 REF

NOTES:

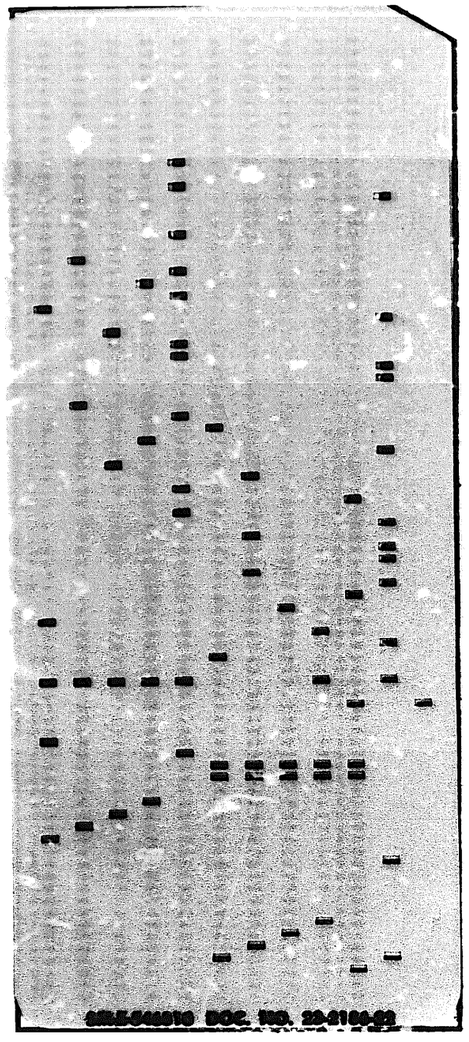
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.



P.C. Assembly SM-E-546810

8 2 P.C. Logic SM-E-546809 Dc . No. 23- 2186-22



TEST PARAMETERS			
Vcc	+4.75V	SIG V	+5EXT @ GRD
+V	—	LOAD REF V	GRD
+V	—	CLK	1 μ sec
-V	—	INT CLK	+5SC

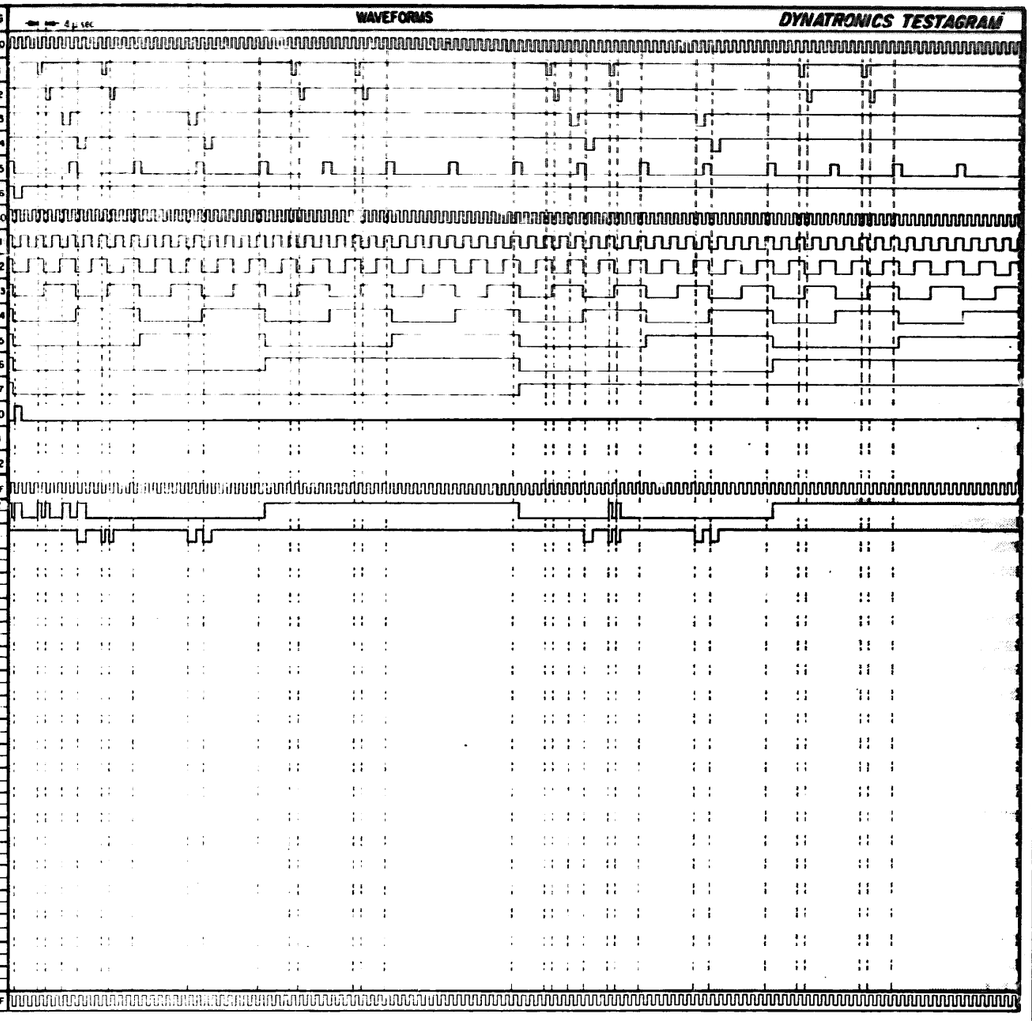
ROW ASSIGNMENT	
10	+S0
1	+B4
2	+B5
3	+B6
4	+B7
5	GRD
6	+C1
7	+C2
8	+C3
9	+C4

OUTPUT PINS (TEST POINTS)
35
41

INPUT PINS	COL	SIG
	63	+C0
31*, 34*	64	-C1
29*, 30*	65	-C2
15*, 31*	66	-C3
23*, 49*	67	-C4
	68	+C5
	69	+C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
50	74	+B4
48	75	+B5
45, 42, 37	76	+B6
52, 33	77	+B7
47, 39	78	+S0
	79	+S1
	80	+S2

SWITCH SETTING

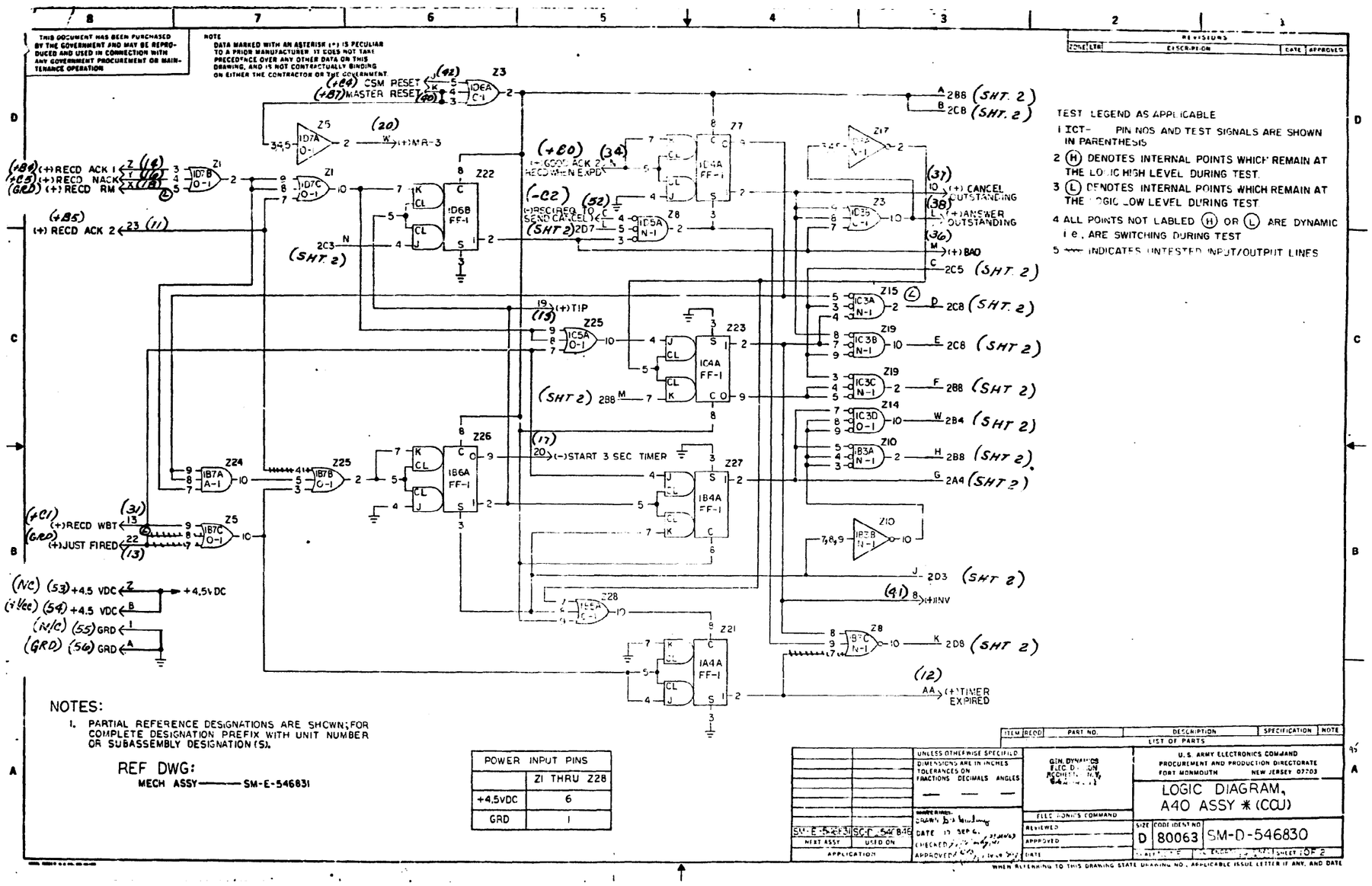
A	1	2	3	4	5	6	7	8	9	10	11	12
B	2	3	7	4	6	8	10	5	9	2	6	9
A	1	2	3	4	5	6	7	8	9	10	11	
B	2	6	3	5	7	9	3	7	11	4	5	



NOTES:

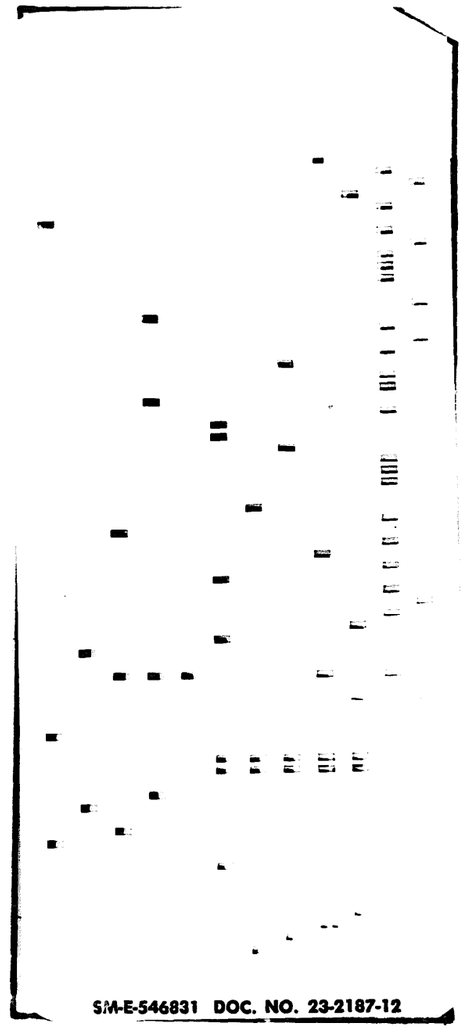
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

GOVT APPD. JN DATE 7-7-71



PC Assembly SM-E-546831

PC Logic SM-D-546830



SM-E-546831 DOC. NO. 23-2187-12

TEST PARAMETERS

V_{cc}	+4.75V	BIT	
±V	—	LOAD REF V	
+V	—	CLK	1 µS
-V	—	INT CLK	÷OSC

ROW ASSIGNMENT

0	+B4
1	+B5
2	+B6
3	+B7
4	+B0
5	—
6	+C1
7	+C*
8	-C2
9	+C3

INPUT PINS	COL	SIG
	63	+C0
24*, 31*	64	-C1
52	65	-C2
	66	-C3
42*	67	-C4
16	68	+C5
	69	-C6
33, 34, 46, 51	70	+B0
	71	+B1
	72	+B2
	73	+B3
14, 50	74	+B4
11, 44	75	+B5
28, 35	76	+B6
48	77	+B7
	78	+S0
	79	+S1
	80	+S2
	*	COM REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
47	
(49)	
(32)	
29	
25	
(15)	
30	
43	
36	
37	
38	
12	
41	
17, 19*	
20	
27	
45	
21	

+ 80 REF

WAVEFORMS — 4 µ S

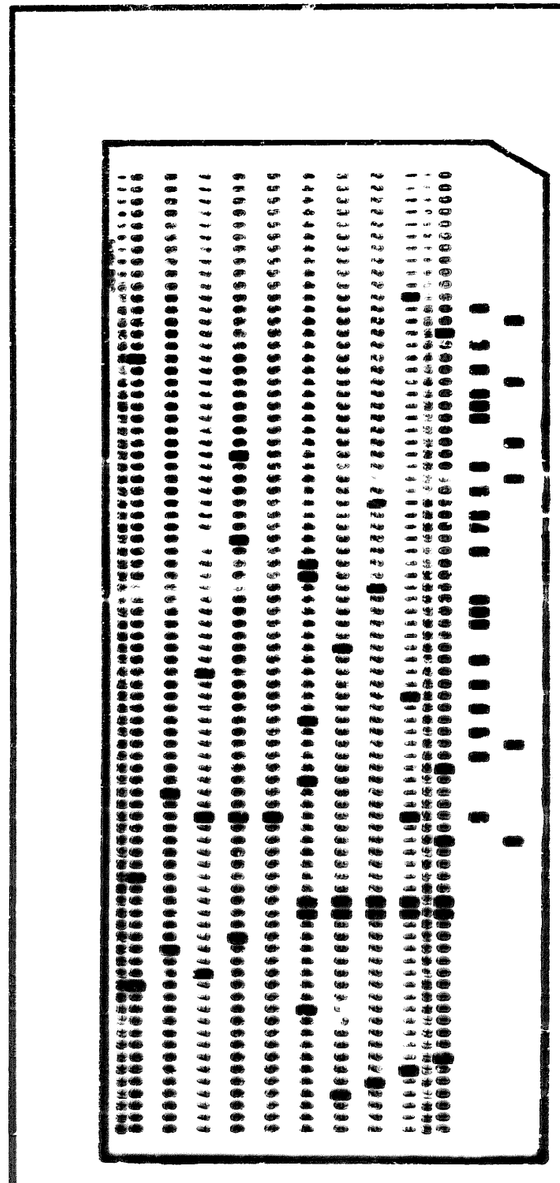
DYNATRONICS TESTAGRAM

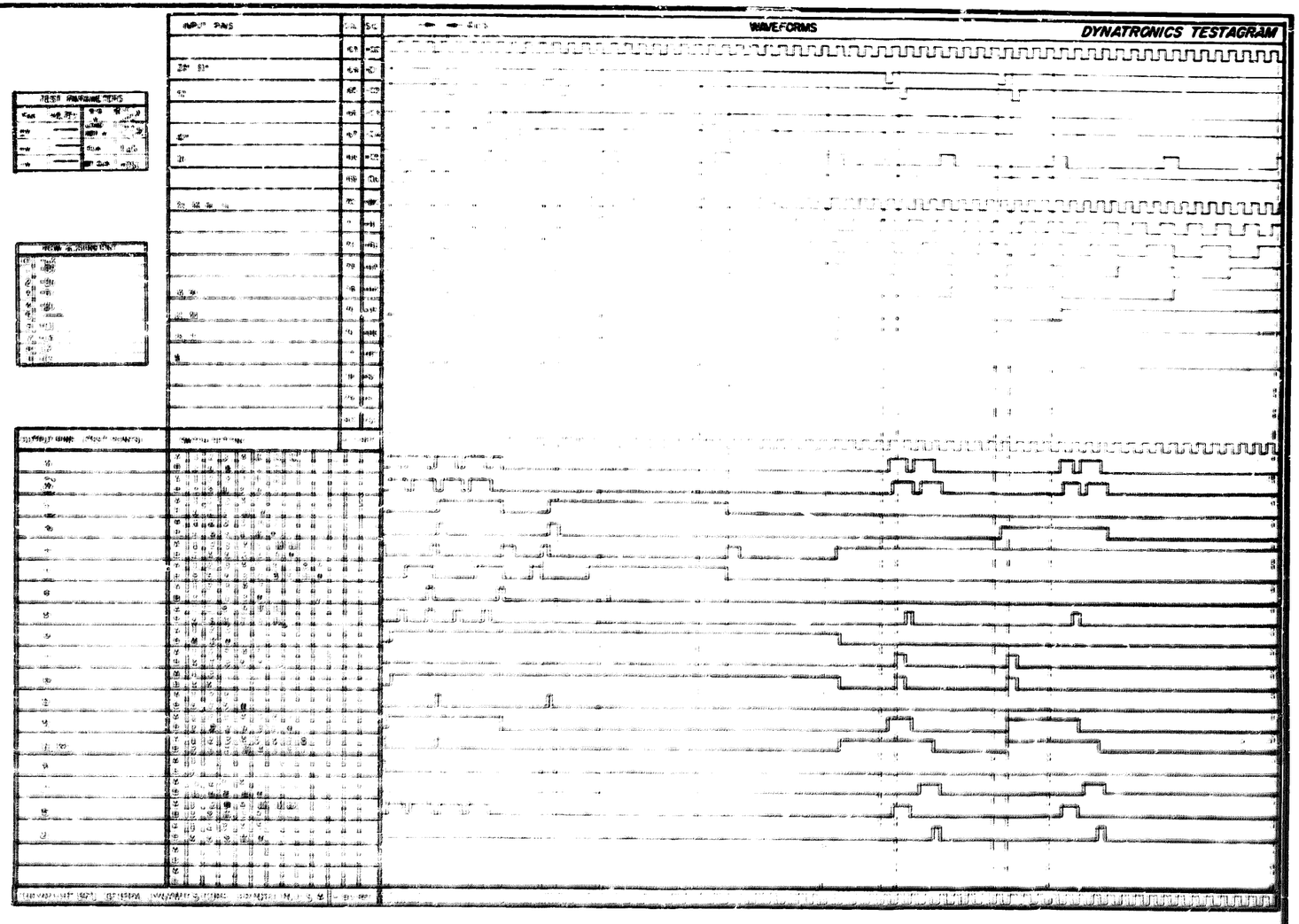
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENICRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

GOVT APPD. JN DATE 5-19-71





NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN DCT-112 TESTER '*' DENOTES ALL POSITIONS OF 'P' SWITCH ARE NO-GO FOR VALID TEST.

   IN DCT-110 TESTER THE [illegible] SWITCH '*' [illegible] IN LOCATED BY '*' [illegible] VERIFICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

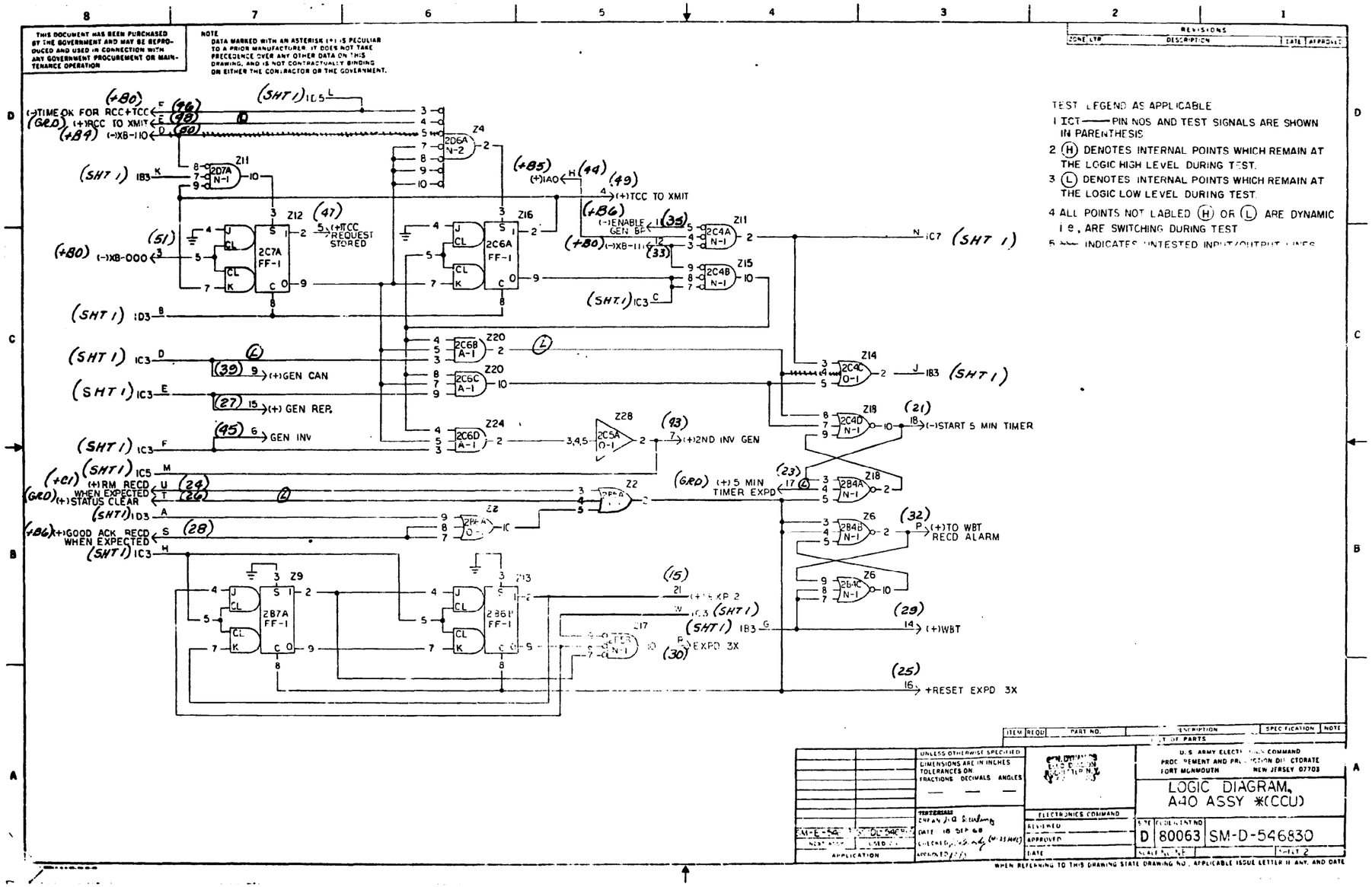
GOVT APPD. JW DATE 6-17-71

DUPLICATE WAVEFORM

Doc. No. 23-2187-12

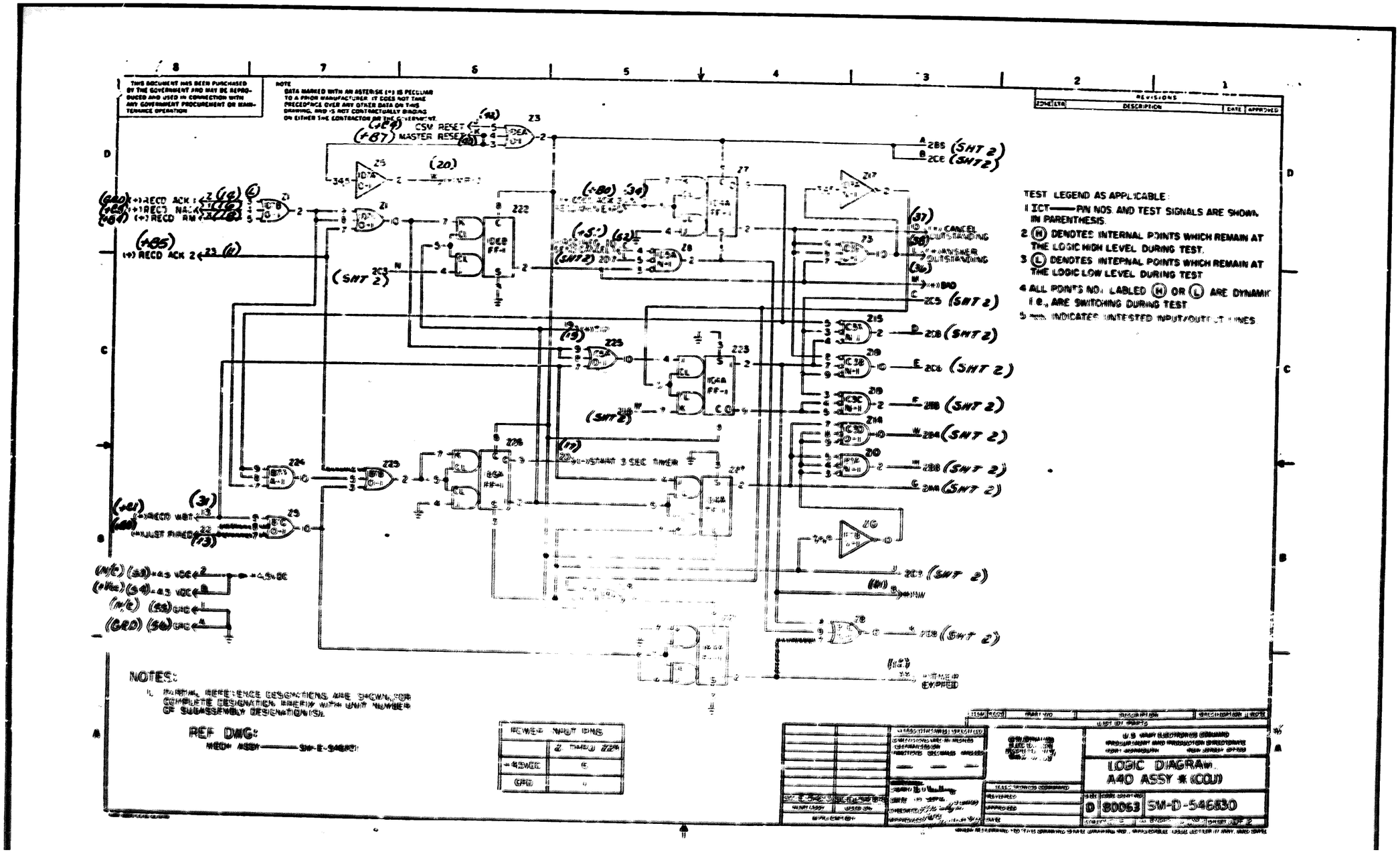
PC Assembly SM-E-546831

PC Logic SM-D-546830



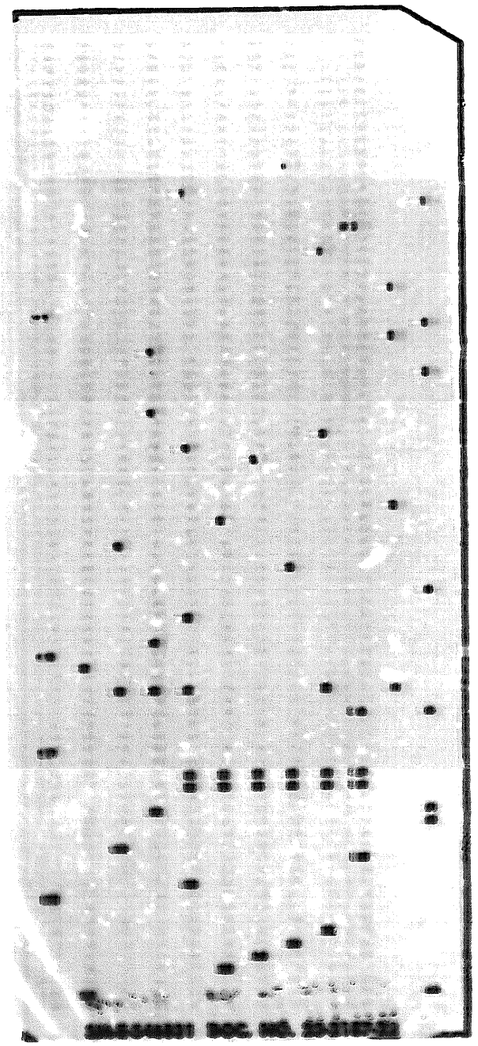
PC Assembly SM-E-546831

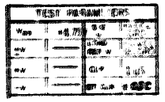
PC Logic SM-D-546830

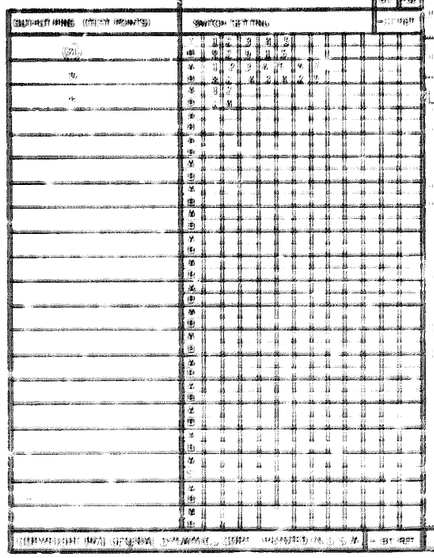


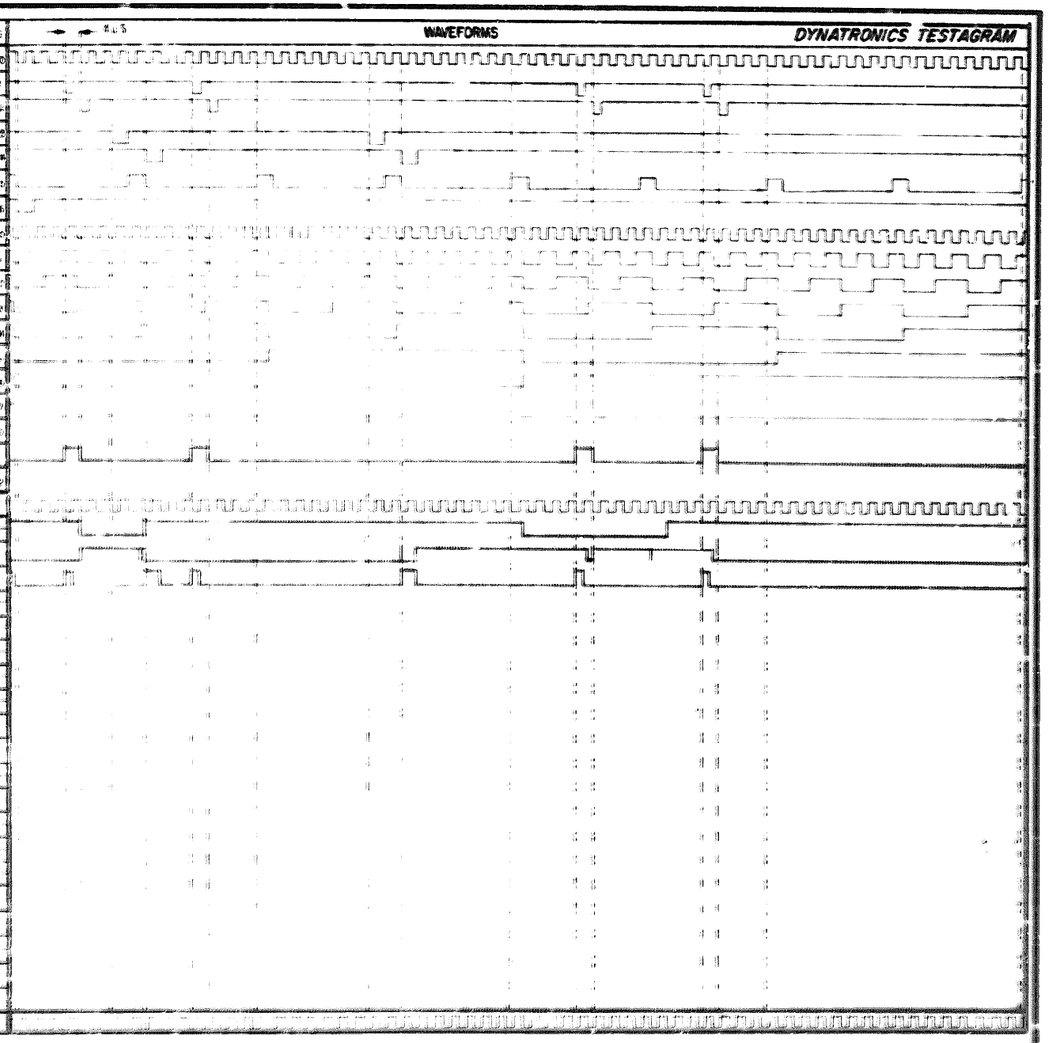
PC Assembly SM-E-546831

 PC Logic SM-D-5468730 Doc. No. 23-2187-22









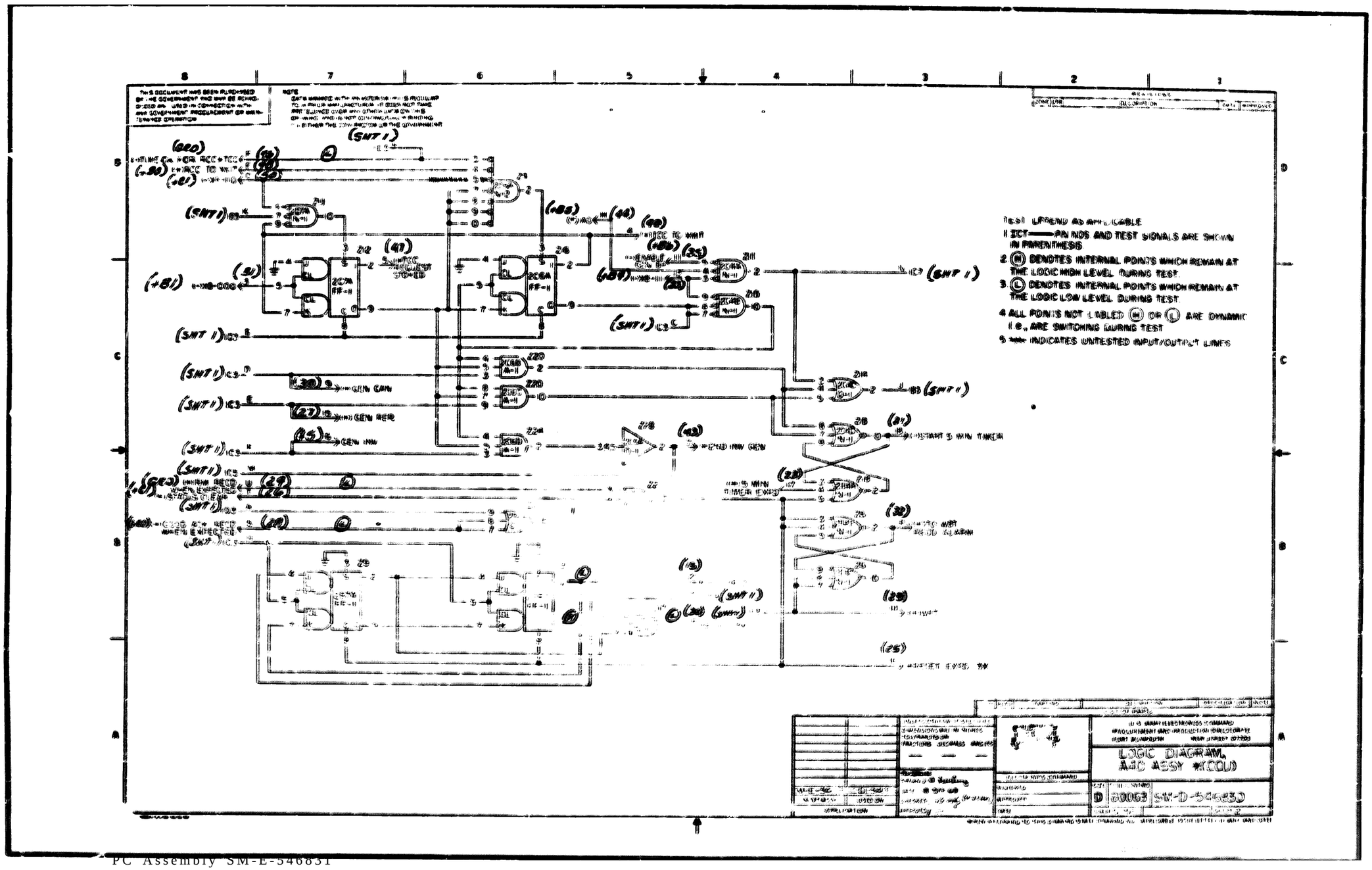
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (-5EXT) LOGIC SUPPLY ADJUSTED TO -4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

GOVT APPD. _____ DATE 6-19-74

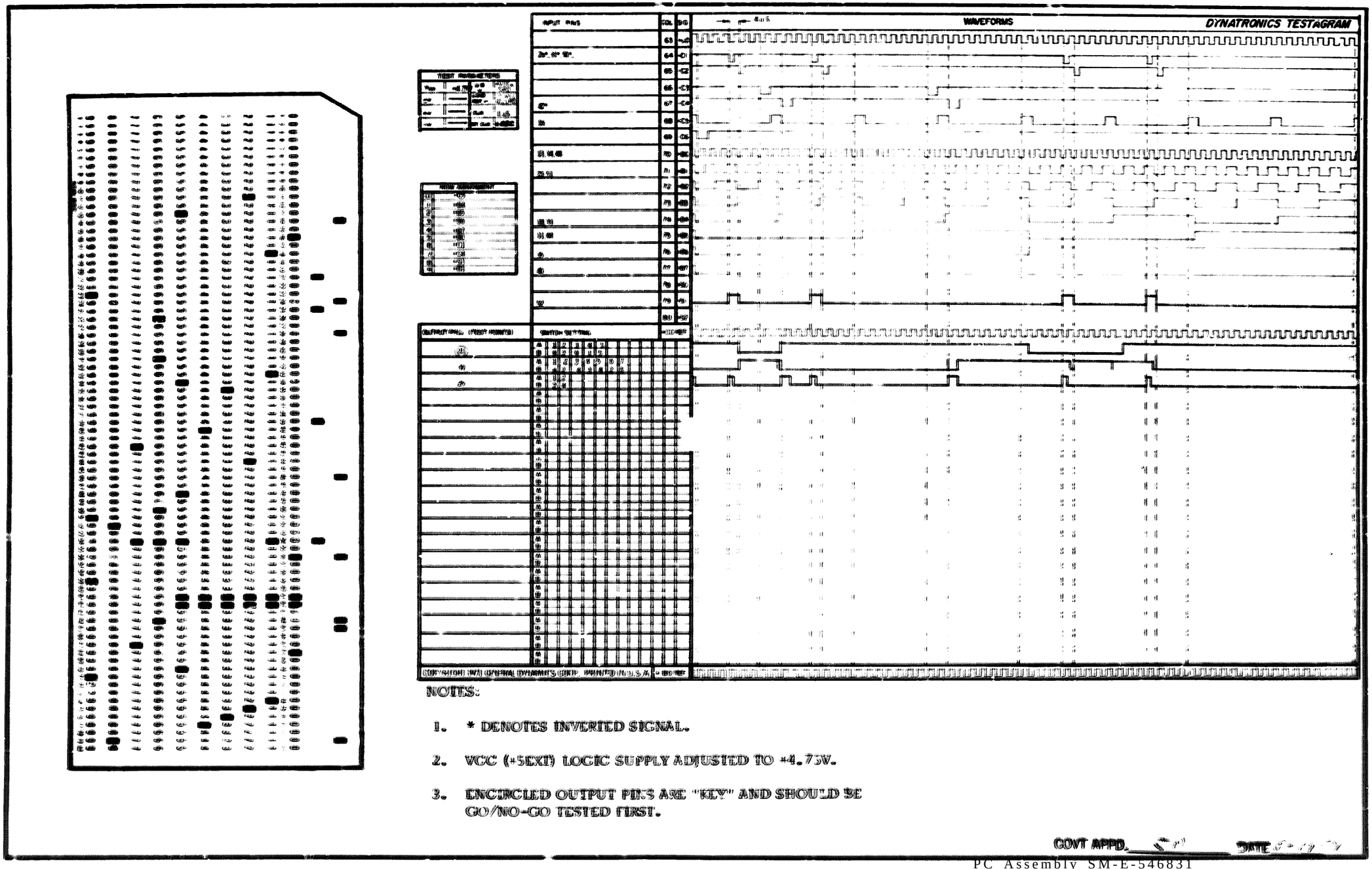
SM-E-546831

546830



PC Assembly SM-E-546831

9 0 PC Logic SM-D-546830 Doc. No. 23-2187-22

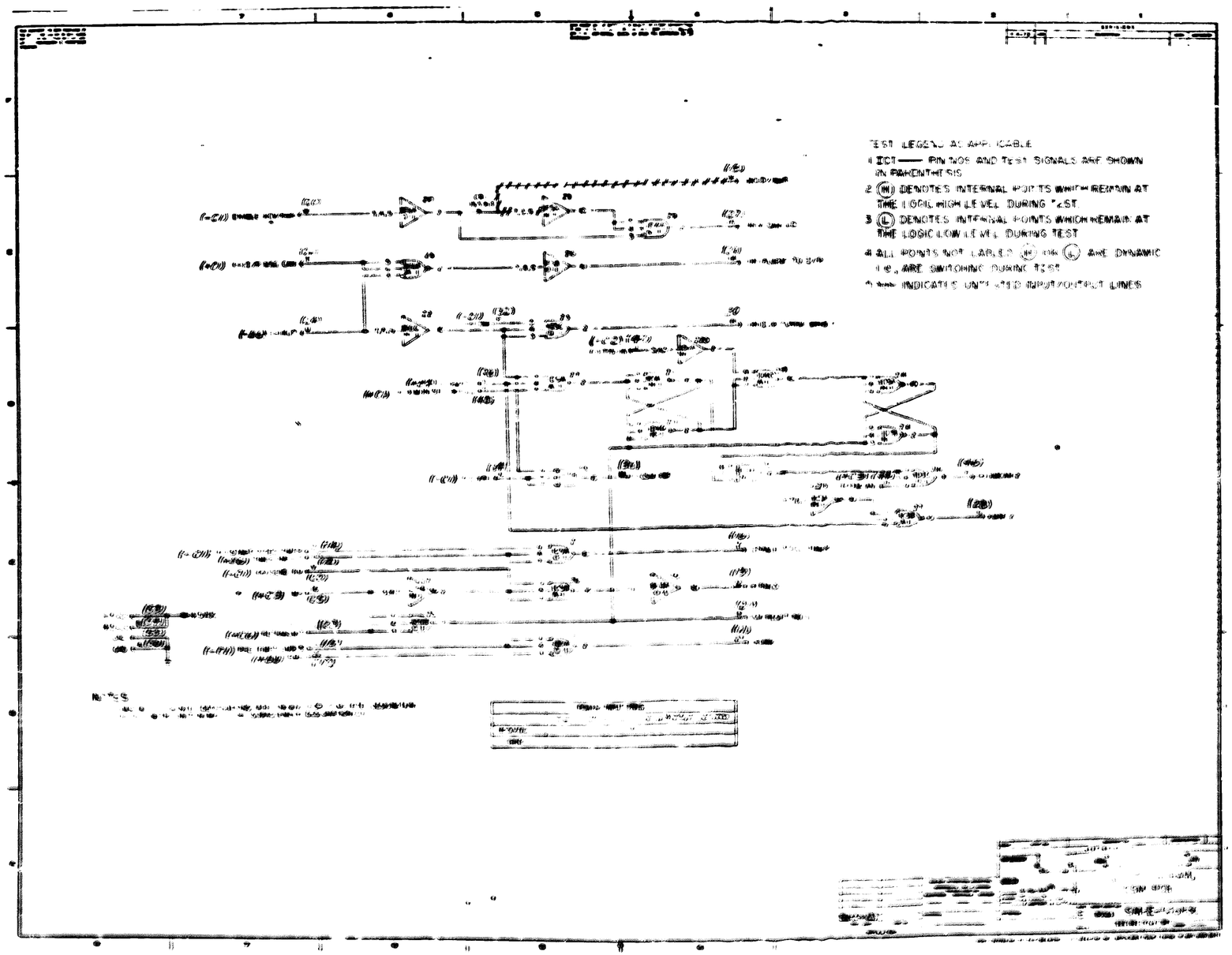


NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

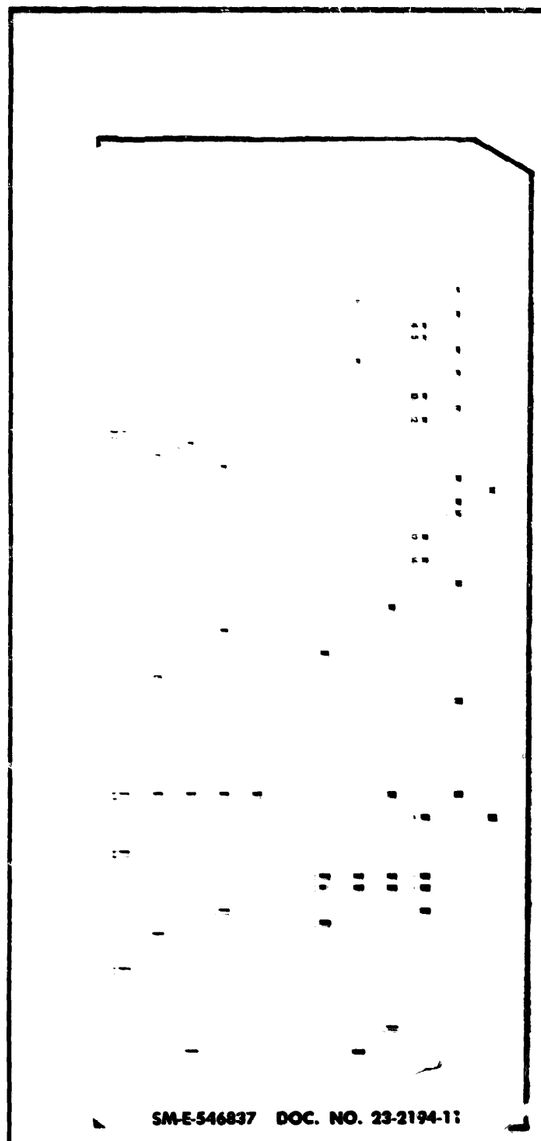
COVT APPD. _____ DATE _____

DUPLICATE WAVEFORM



P.C. Assembly SM-E-546837

P.C. Logic SM-E-546836 Doc. No. 23-2391-1



SM-E-546837 DOC. NO. 23-2194-11

GOVT APPD. JN DATE 2-2-72

TEST PARAMETERS			
V_{CC}	+4.75V	SIG LOAD REF V	+SC1, GRD, 1½ VCC
+V	—	CLR	1 μ SEC
-V	—	INT CLR	+OSC

ROW ASSIGNMENT	
10	-C1
1	-B4
2	+B2
3	-C2
4	—
5	—
6	+C1
7	-B0
8	+C3
9	+C0

INPUT PINS	COL	SIG
	63	+C0
20, 26, 32, 40, 34, 14, 27, 15	64	-C1
47	65	-C2
44, 25	66	+C3
	67	-C4
	68	+C5
23	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
18	74	+B4
	75	+B5
24, 17, 17	76	+B6
	77	+B7
	78	+S0
	75	+S1
	80	+S2
	+20 REF	

OUTPUT PINS (TEST POINTS)

11, 10, 30, 36, 29

28

(50)

13

21

27

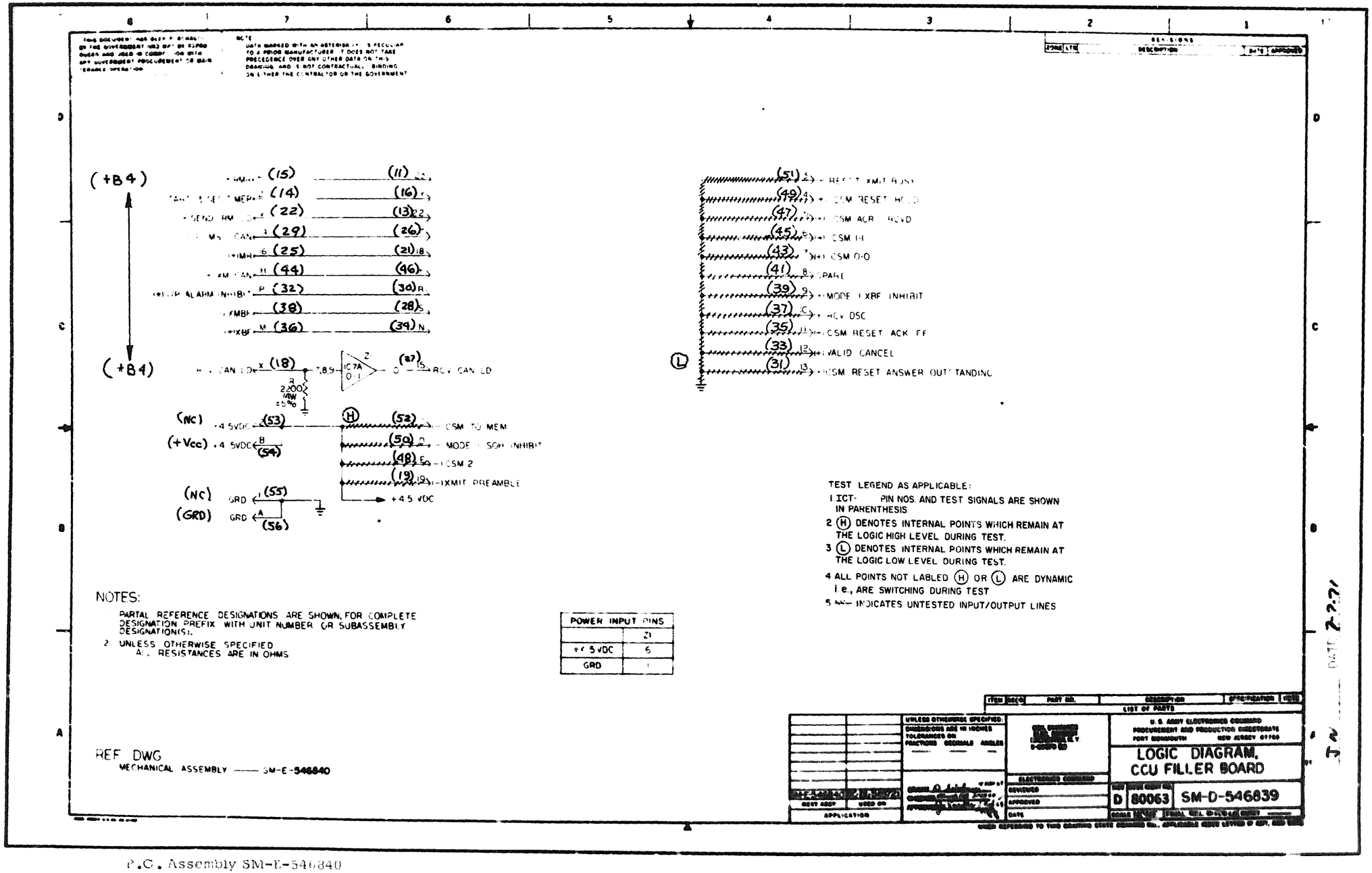
SWITCH SETTING

WAVEFORMS — 4 μ SEC.

DYNATRONICS TESTAGRAM*

NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.



P.C. Assembly SM-E-546840
P.C. Logic SM-E-546839

TEST PARAMETERS

Vcc	+4.75	SIG V	GRD +VCC
±V	—	LOAD REF V	11, VCC
+V	—	CLK	1 µ sec
-V	—	BIT CLK	+OSC

ROW ASSIGNMENT

10	—
1	—
2	—
3	—
4	—
5	—
6	+B4
7	—
8	—
9	—

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
14, 15, 18, 22, 25, 29, 32, 36, 38, 44	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

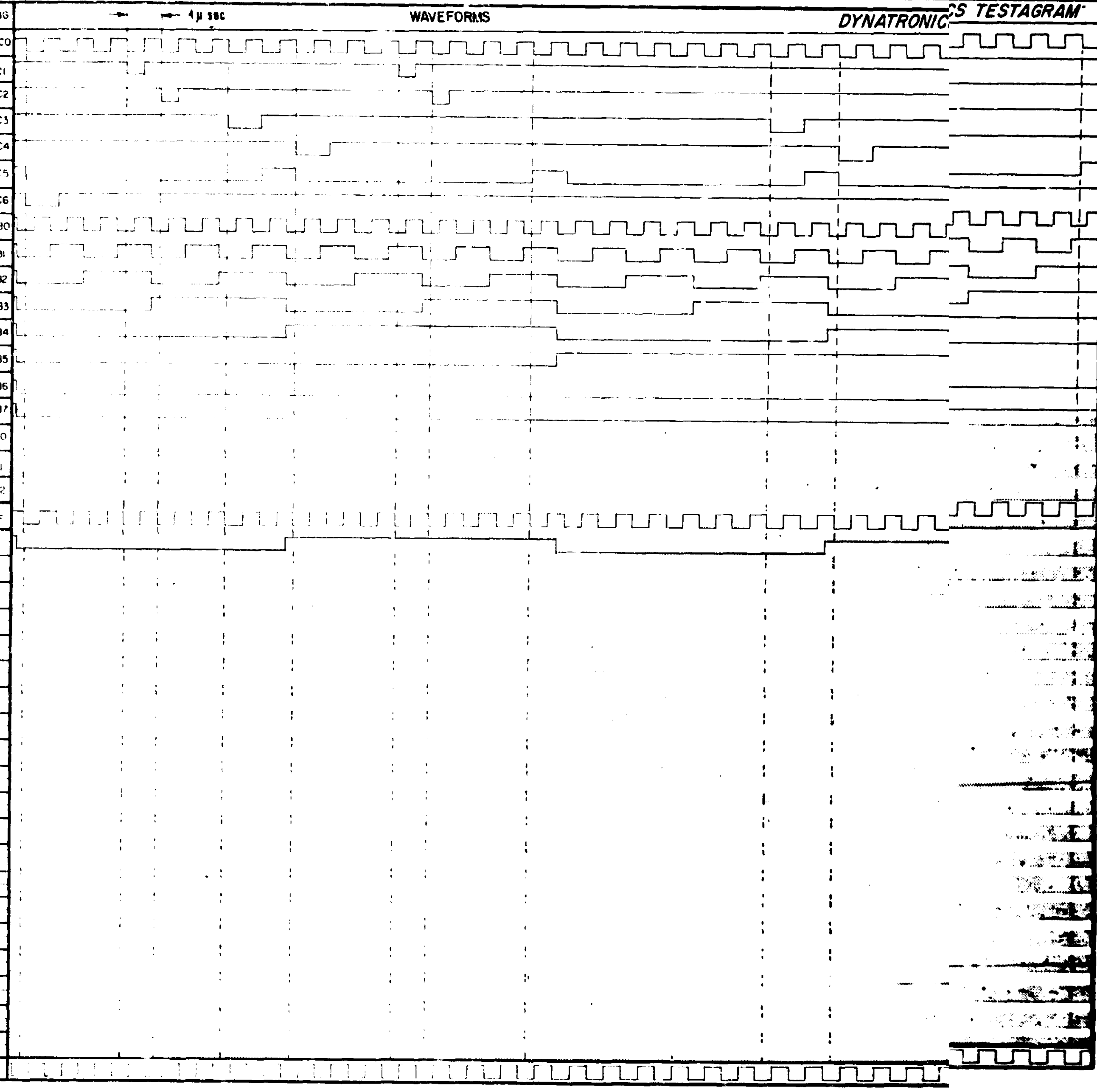
OUTPUT PINS (TEST POINTS)	SWITCH SETTING				
11, 13, 16, 21, 26, (27), 28, 30, 34, 46	A / B	1 / 2	2 / 1	3 / 11	4 / 10

+C0 REF

+B0 REF

WAVEFORMS

DYNATRONICS TESTAGRAM

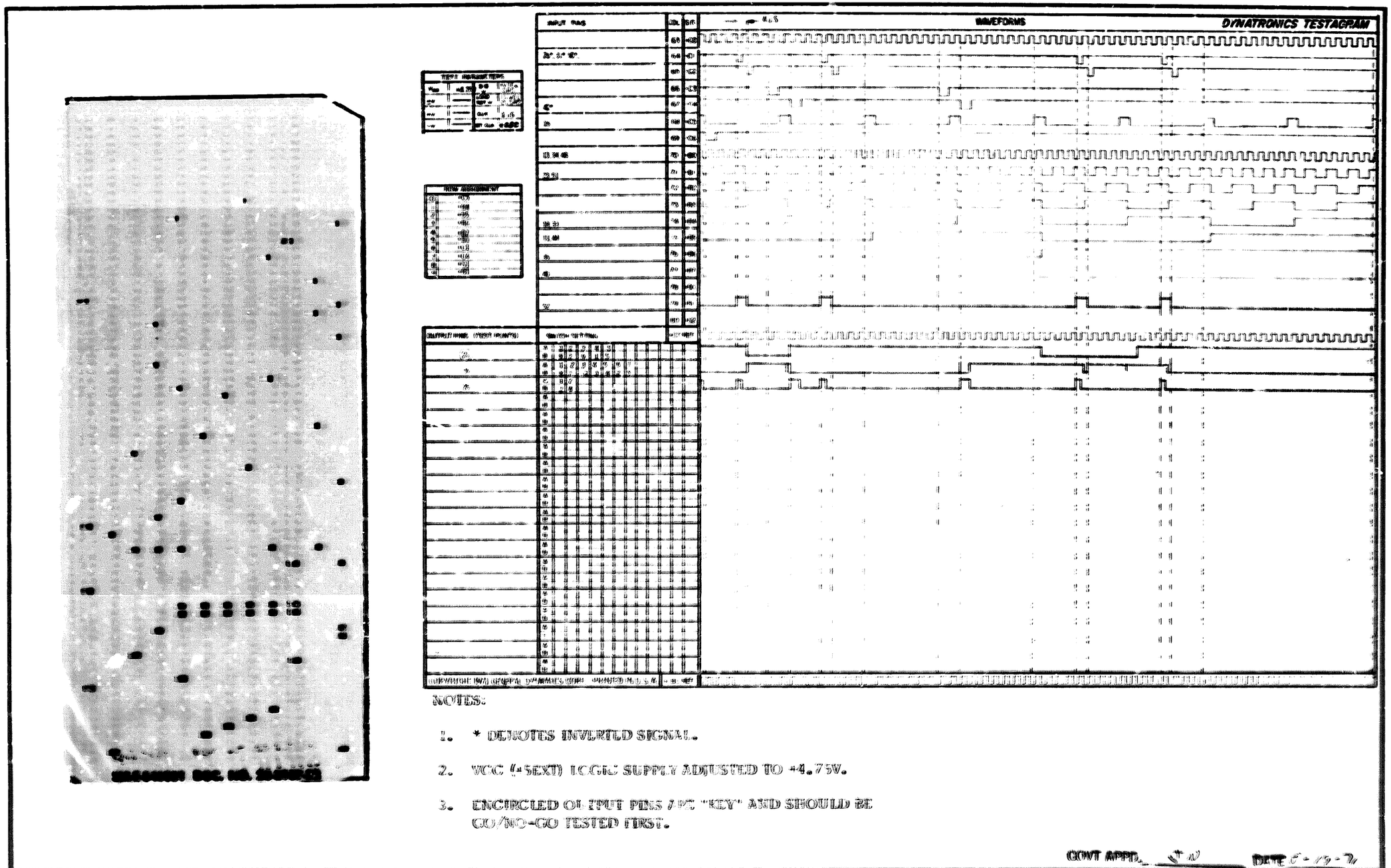


NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

SM-E-546840 DOC. NO. 23-2188-11

GOVT APPD. JN DATE 7-7-71



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OR INPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

GOVT APPD. _____ DATE 6-19-72

PC Assembly SM-E-546831

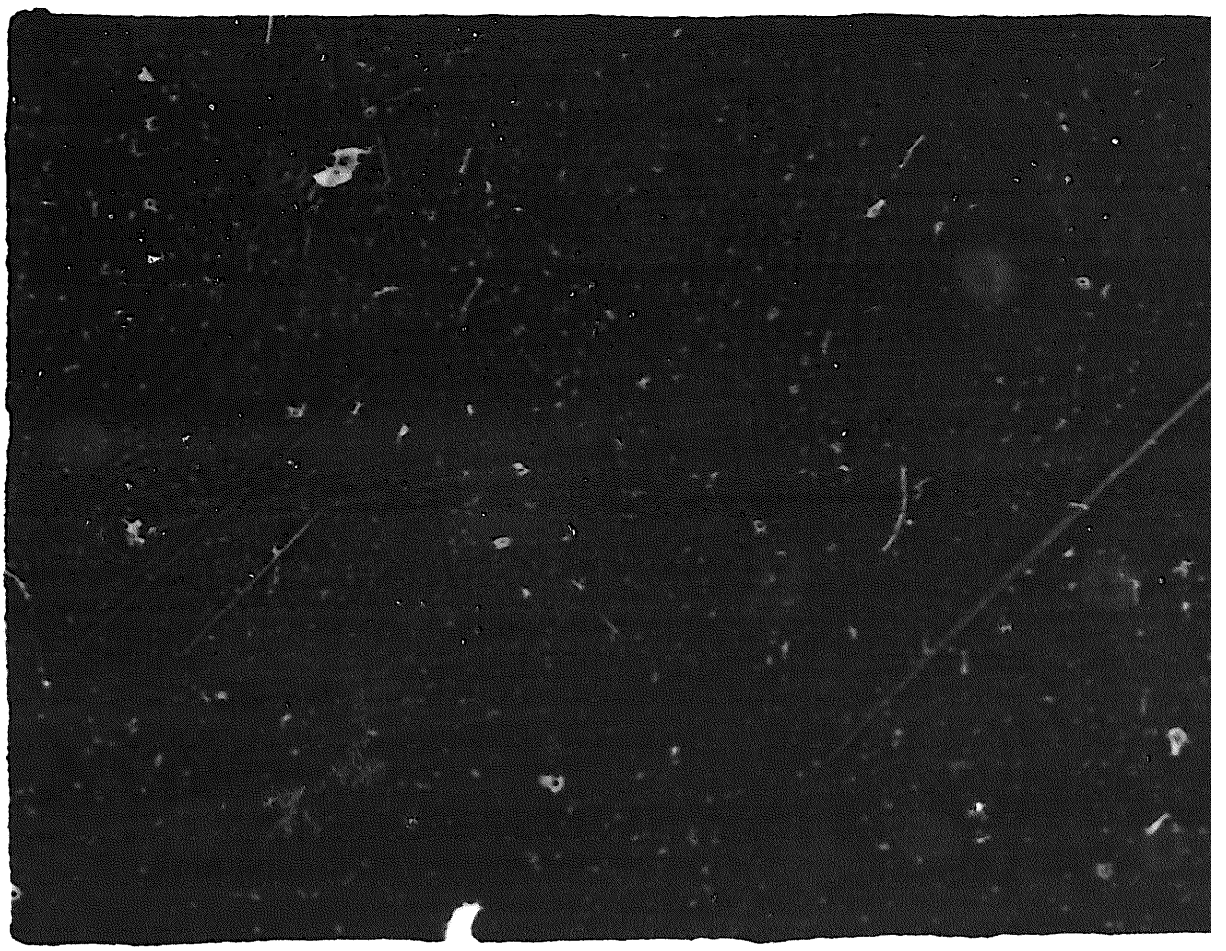
Doc. No. 23-2187-22

PC Logic SM-D-646830

END

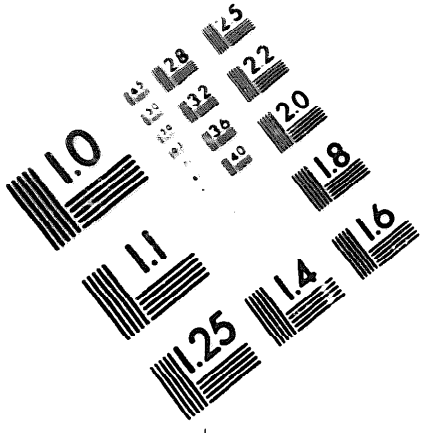
02-05-83

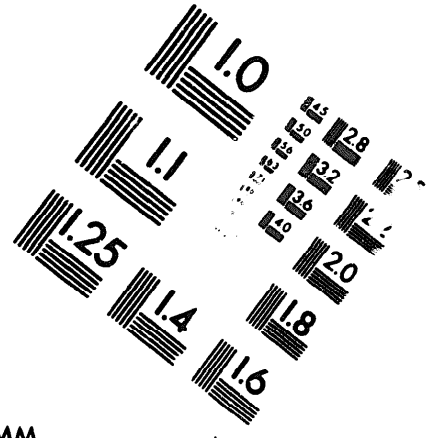
DATE



DEPARTMENT OF THE ARMY

MICROFORM
TEST TARGET





150 MM

1.0 mm (e= .81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

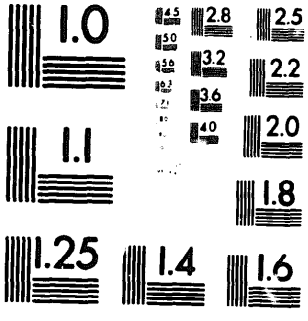
ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*



1.0 mm (e= .81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

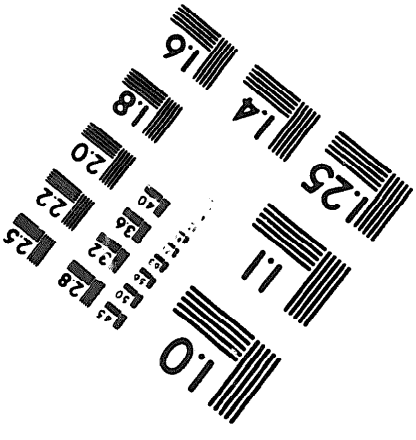
2.0 mm (e= 1.37 mm)

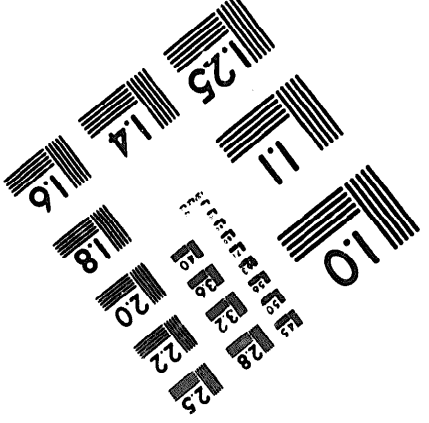
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

200 MM





250 MM